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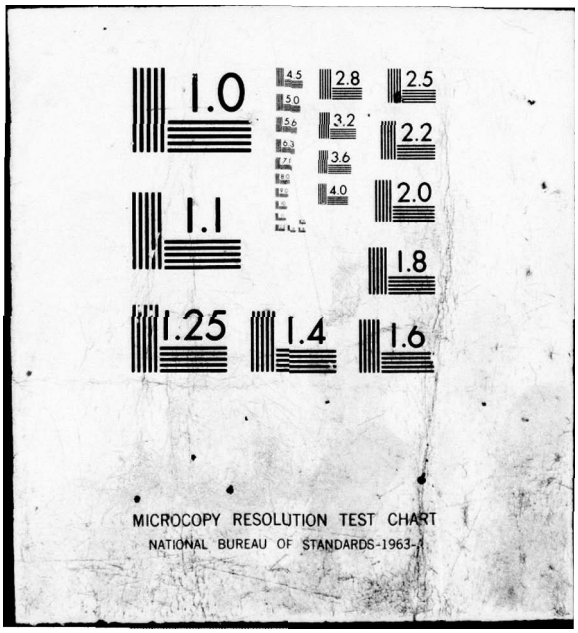
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Technical Report 498

HIGH-SPEED SPECTRUM-ANALYSIS TECHNOLOGIES

K Bromley

January 1980

Final Report: January — September 1978

Prepared for
Rome Air Development Center

Approved for public release; distribution unlimited

NAVAL OCEAN SYSTEMS CENTER
SAN DIEGO, CALIFORNIA 92152

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Commander

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Techniques and technologies for performing frequency decomposition on an input signal in a small-size, low-cost, low-power unit are analyzed. (Typical device parameters of interest are an input signal bandwidth of 2 MHz and a frequency resolution of 4 kHz.) It is found that no present-day technology is capable of satisfying these objectives entirely, but that incoherent optics technology, particularly the electro-optical processor under development at NOSC, and electronic CCD technology, particularly the chirp-Z transform, both have high potential for doing so.

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SUMMARY

OBJECTIVE

Analyze techniques and technologies for performing frequency decomposition (i.e., Fourier transformation) on an input signal in a small-size, low-cost, low-power unit. (Typical device parameters of interest are an input signal bandwidth of 2 MHz and a frequency resolution of 4 kHz.)

RESULTS

1. No technology satisfies the stated objective with its present day state-of-the-art.

2. Digital FFT circuits using high-speed A/D converter and multiplier chips meet the small-size and low-cost requirements and come within a factor of 4 of the speed specification but are power consumptive.

3. Incoherent optics technology, particularly the electro-optical processor under development at NOSC, and electronic CCD technology, particularly the chirp-Z transform devices developed at Reticon and Texas Instruments, both have high potential for meeting the stated requirements with some further development.

4. The remaining technologies investigated are clearly inadequate in that a major technology breakthrough would be required to cost-effectively meet the desired specification.

RECOMMENDATIONS

1. Continue monitoring the use of digital electronic technology for spectral analysis. It is anticipated that increased throughput and decreased power consumption should be achieved in the near future due to the considerable momentum of the commercial digital electronics field and the advances predicted by DoD's VHSIC program.

2. Support the development of a high-speed DFT module using electro-optical processing (EOP) technology. The use of a custom gated-output CCD now under development at RCA would allow the fabrication of a 128-point DFT analyzer with a throughput rate of 1M real samples per second in FY 80 with high potential for further performance improvement.

3. Support the development of high-speed analog circuitry (either on-chip or external) for performing the pre- and post-multiplications associated with a chirp-Z transform. Electronic CCD devices can meet the desired performance specifications for the crosscorrelation portion of the algorithm with their present state of development.

1. INTRODUCTION

This report summarizes the results of a project entitled "Multiple Channel Application Study" performed by the author for Rome Air Development Center/IRAA during the period 1 March 1978 through 30 September 1978. The following four paragraphs constitute the statement of work for this task:

OBJECTIVE: To investigate and report on the feasibility of determining activity and demodulating of multichannel communication signals (up to 600 channels) in real time.

BACKGROUND: In recent years considerable progress has been made in technology and the use of this technology in the development of complex communication systems. For high-capacity systems (greater than 64 channels) it becomes extremely difficult for an intercept system to monitor, track, and subsequently demodulate the active channels. Recently, it has been realized that there may be important potential uses for optical processing techniques in the field of COMINT. The ability to perform functions such as filtering, demodulation and detection at extremely high rates by means of optical techniques could make possible dramatic performance improvements and in some cases provide entirely new capabilities for real-time signal processing. In addition, the use of high-speed solid state technology offers a potential to provide solutions to the multi-channel communication problem.

EFFORT: A study shall be conducted to determine the feasibility of real-time processing of multi-channel communication signals (up to 600 channels). Various types of technology shall be investigated to determine which techniques will be most effective in solving the problem. These technologies shall include conventional digital electronics, analog electronic devices, incoherent electro-optical processors, and optical processors utilizing fiber optics. Demonstration of the selected technique or techniques is desirable.

DATA ITEM: A report detailing the technology comparisons and recommending specific approaches shall be a deliverable requirement of this effort.

The principal signal processing problem inherent in performing the desired functions of filtering, demodulation, and detection on multichannel communications signals is the operation of spectral decomposition. Once this is done, the channels of interest can each be filtered, demodulated, and/or detected through conventional means. The more mathematical term for spectral decomposition is Fourier analysis. Hence the task becomes one of (1) investigating various techniques and technologies capable of performing Fourier transformations on an input signal in a small-size, low-cost, low-power unit, and (2) making recommendations on the direction of further technology development to make such a unit feasible.

To clearly illustrate the problem limits, the following typical Fourier transformation parameters were selected:

- an input signal bandwidth of 2 MHz,
- a frequency resolution of 4 kHz (i.e., the input signal should be decomposed into approximately 500 channels),
- the use of a good window function (such as a Kaiser-Bessel window), and
- an appropriate percentage of window overlap to achieve the necessary sampling rate for demodulation (typically 50%).

These are intended simply as a common set of parameters for use in comparing various techniques and states-of-the-art and are not meant to be restrictive or necessarily descriptive of a specific application.

The next section will define the Fourier transform operation and provide a mathematical basis into which we can insert these desired parameters. While the main thrust of

this report is a technology comparison, this digression into theory and equations is necessary if ambiguities in terminology are to be avoided. With that task completed, the subsequent sections will utilize this framework in quantitatively assessing the ability of the various signal processing technologies currently under development to satisfy these demands.

In the comparison of various technologies, several specific commercially available devices will be discussed as illustrations of the state-of-the-art, and advertising literature and specifications sheets are included as an aid to the reader. This should not be interpreted as an endorsement by DoD of these products or their manufacturers.

2. THE DISCRETE FOURIER TRANSFORM

This brief section on the Fourier transform utilizes some familiar results from linear systems theory to specify a set of parameters to be utilized in subsequent discussions. No attempt is made here to derive any of these results. The unfamiliar reader can consult any of several excellent texts on linear systems theory, digital signal processing, and Fourier analysis (Refs. 1, 2, 3).

The continuous Fourier transform is a relationship between a function of time (or space, in optical systems) and a function of temporal frequency (or spatial frequency). That is, given the input function g(t), its Fourier transform is

$$G(f) = \int_{-\infty}^{\infty} g(t)\, e^{-2\pi i f t} dt \quad . \tag{1}$$

Conversely, given G(f), the inverse Fourier transform of G(f) is

$$g(t) = \int_{-\infty}^{\infty} G(f)\, e^{2\pi i f t} df \quad . \tag{2}$$

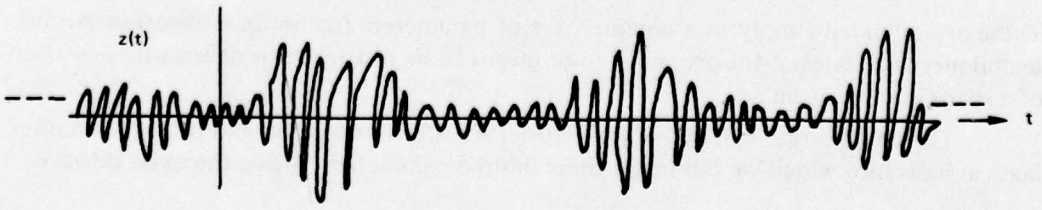
The unit of t is seconds and the unit of f is cycles per second (or hertz). These equations define a relationship between two different ways of visualizing a signal: either its conventional temporal direct waveform, g(t), or its temporal-frequency representation, G(f), which denotes the amplitudes and phases of every sinusoidal component of g(t).

In more graphical terms, Eqs. (1) and (2) relate a function in time space to its equivalent function in frequency space, i.e.,

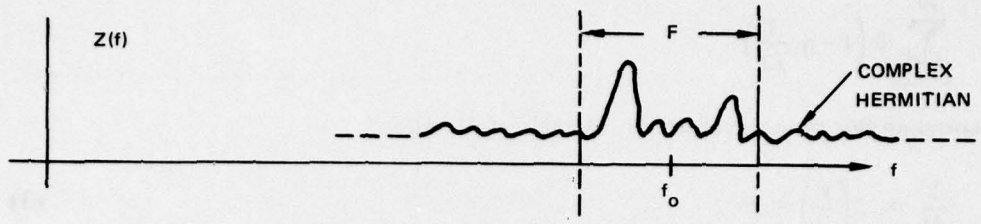
where the symbol ⇔ denotes the Fourier transform relationship.

A. COMPLEX ANALYSIS

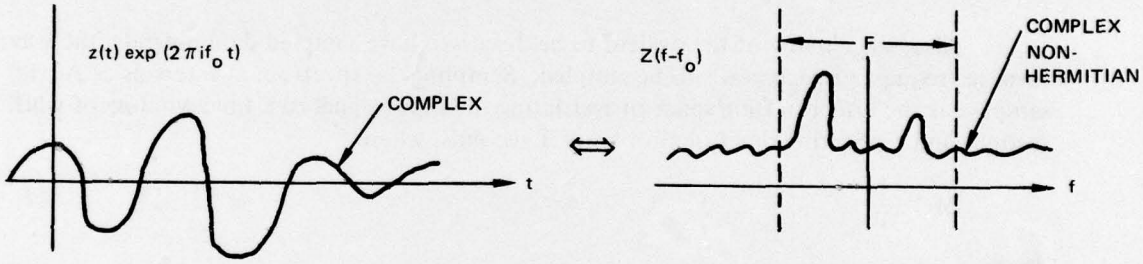
Let us suppose that the input signal to the receiver, as received at the antenna, is given by z(t); i.e., it is a real continuous temporal waveform.



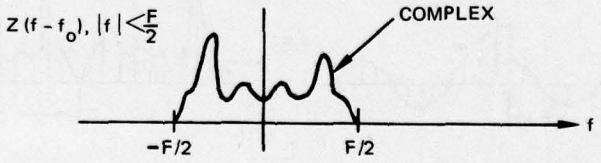
The Fourier transform, Z(f), of such a waveform is a complex continuous waveform in frequency space. It is Hermitian (i.e., real part is even, imaginary part is odd) due to z(t) being real. Let us stipulate that due to some *a priori* knowledge of the nature of z(t), only the region of total bandwidth F, centered on the frequency f_o, is of interest.



Since many of the technologies to be investigated in the next chapter are sampled-data systems, the input signal must be sampled before being processed. If z(t) is sampled directly, then the Nyquist sampling theorem states that z(t) must be sampled at at least twice the highest frequency; hence the sampling frequency would have to be at least $2(f_o + F/2)$. But since the total bandwidth of interest is only of width F, this is obviously inefficient. It makes much better sense to first baseband the frequency region of interest. This is accomplished by multiplying z(t) by $\exp(2\pi i f_o t)$, which has the effect of shifting Z(f) to the left by the amount f_o. Note that $z(t) \exp(2\pi i f_o t)$ is not a real function and hence its Fourier transform, $Z(f - f_o)$, is not Hermitian.



The next step is to pass the basebanded signal through a low-pass filter that transmits only the frequency components $|f| \leq F/2$. This yields a waveform which, in frequency space, looks like



Sampling this waveform at the Nyquist limit yields a sampling frequency of 2(F/2).

The term "sampling the waveform" means multiplying that waveform by a sequence of Dirac delta functions (normalized by the width Δt):

$$\Delta t \sum_{n=-\infty}^{\infty} \delta (t - n \Delta t) \ .$$

By the convolution theorem, multiplication in time space implies convolution in frequency space. Therefore the Fourier transform of the waveform must be convolved with the Fourier

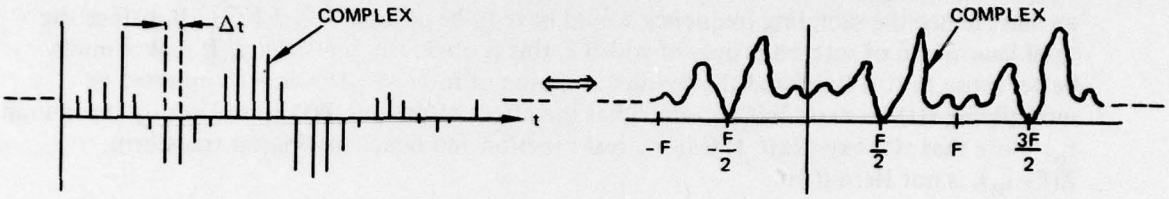
transform of the delta function sequence, which can be shown to be also a sequence of Dirac delta functions, namely,

$$\sum_{n=-\infty}^{\infty} \delta\left(f - n\,\frac{1}{\Delta t}\right) .$$

Thus sampling this time waveform at intervals of Δt, where

$$\frac{1}{\Delta t} = 2\left(\frac{F}{2}\right) = F \quad , \tag{3}$$

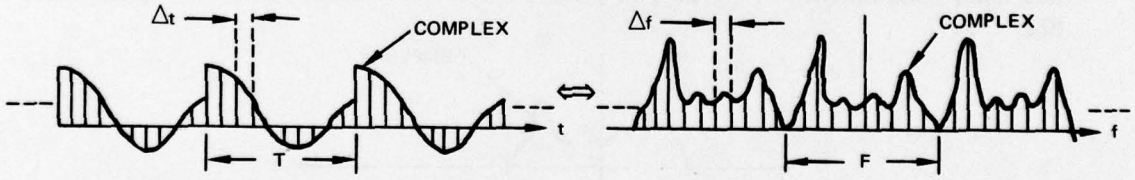
has the effect in frequency space of replicating the frequency waveform about multiples of F.



Also, since many of the devices to be discussed have sampled-data outputs, the waveform in frequency space needs to be sampled. Sampling the spectrum at intervals of Δf Hz/sample has the effect in time space of restricting the input signal to a time window of width T seconds and replicating this function every T seconds, where

$$\Delta f = \frac{1}{T} \quad . \tag{4}$$

That is



Since the time-space and frequency-space representations both completely characterize the same physical signal, there must be an equal number of "variables" or samples in each representation. One can think of this as a conservation of the number of degrees of freedom. Let this number be N. Thus

$$N = \frac{T}{\Delta t} = \frac{F}{\Delta f} \quad . \tag{5}$$

Since by sampling in time and frequency the processing task has been changed from a continuous one to a discrete one, the integral formulation of Eqs. (1) and (2) becomes the discrete Fourier transform (DFT) operation of

$$G_m = \sum_{n=1}^{N} g_n \exp\left(-2\pi i\,\frac{mn}{N}\right) \tag{6}$$

and

$$g_n = \sum_{m=1}^{N} G_m \exp\left(2\pi i \frac{mn}{N}\right) \tag{7}$$

where n and m denote sample numbers in time space and frequency space, respectively.

All that remains of this analysis now is to insert the desired typical parameters from Section 1 into Eqs. (3), (4), and (5) to characterize the form of the required Fourier transformer.

If the input signal bandwidth of interest is

$$F = 2.048 \text{ MHz} \tag{8}$$

then by Eq. (3) the required temporal sampling period is

$$\Delta t = \frac{1}{F} = 0.488281250\ \mu s \ . \tag{9}$$

If the frequency resolution of interest is

$$\Delta f = 4 \text{ kHz} \tag{10}$$

then by Eq. (5) the number of complex samples to be utilized is

$$N = \frac{F}{\Delta f} = \frac{2.048 \text{ MHz}}{.004 \text{ MHz}} = 512. \tag{11}$$

Inserting these two results into Eq. (4) yields the total integration time (or window length) required as

$$T = N\,\Delta t = 250\ \mu s \ . \tag{12}$$

As discussed extensively in Ref. 4, it is beneficial to apply a window function, w(t), to the input signal either before or during the DFT operation in order to reduce the frequency sidelobes below the -13-dB level for the rectangular window (i.e., no window function at all) assumed so far in these calculations. Reference 4 lists several choices and quantitatively assesses the trade-offs involved. It shows many plots of desirable window functions w(t) and their Fourier transforms W(f). The multiplication of the input data by one of these window functions effectively gives very little weighting to the input sample points near the ends of the window. Hence, it is necessary to use some overlap factor in calculating the DFT's so that all input samples are taken into account. The most commonly used overlap factor is 50%. Using the parameters just calculated, the desired processor must transform a 250-μs window of the input signal, g_n, every 125μs. That is, every 125 μs it must read in 512 complex input samples and generate 512 complex output spectral samples. The effective throughput rate is therefore

$$\frac{512 \text{ complex samples}}{125\ \mu s} = 4.096 \text{ M } \frac{\text{complex samples}}{\text{second}} \ . \tag{13}$$

In summary, the required Fourier transformer has as its input

$$g_n \equiv g(n\,\Delta t) = z(t) \cdot \exp(2\pi i f_o t) \cdot w(t) \cdot \Delta t \sum_{n=-\infty}^{\infty} \delta(t - n\,\Delta t) \otimes \sum_{m=-\infty}^{\infty} \delta(t - mT) \tag{14}$$

and produces as its output

$$G_m \equiv G(m\,\Delta f) = Z\left(f - f_o\right) \otimes W(f) \otimes \sum_{n=-\infty}^{\infty} \delta(f - nF) \cdot \Delta f \sum_{m=-\infty}^{\infty} \delta(f - m\,\Delta f) \quad (15)$$

where the symbol $\otimes$ denotes convolution. It must perform this operation with input rates for g_n and output rates for G_m of approximately 4 million complex samples per second.

B. REAL ANALYSIS

While some of the technologies to be discussed (e.g., coherent optics and digital electronics) are capable of processing the complex input data stream described above, several others (e.g., incoherent optics and CCD's) are restricted to real input signals and real operations. Fortunately, the DFT operation can still be performed by such devices by processing the two real components comprising each complex quantity separately. The equations can be written by simply inserting the identities

$$\exp(-2\pi\,\mathrm{ift}) = \cos(2\pi\,\mathrm{ft}) - \mathrm{i}\sin(2\pi\,\mathrm{ft}) \quad (16)$$

and

$$\exp(2\pi\,\mathrm{ift}) = \cos(2\pi\,\mathrm{ft}) + \mathrm{i}\sin(2\pi\,\mathrm{ft}) \quad (17)$$

into Eqs. (1) and (2) and requiring that the input signal, g(t), be real. The latter requirement can be insured through reconfiguring the receiver processing as follows: Instead of base-banding the received signal z(t) as before, perform the following three operations:

1. Pass z(t) through a bandpass filter to retain only those frequency components of interest, namely

$$f_o - \frac{F}{2} \leqslant |f| < f_o + \frac{F}{2}$$

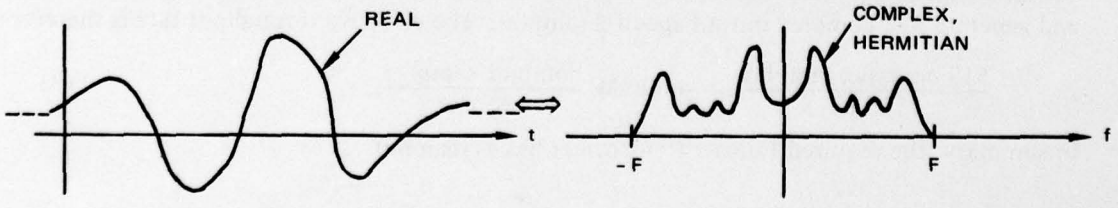
2. Multiply this waveform by

$$\cos\left[2\pi\left(f_o - \frac{F}{2}\right)\right]$$

3. Pass the resulting real waveform through a low-pass filter to retain only those components within

$$-F \leqslant |f| < +F \quad .$$

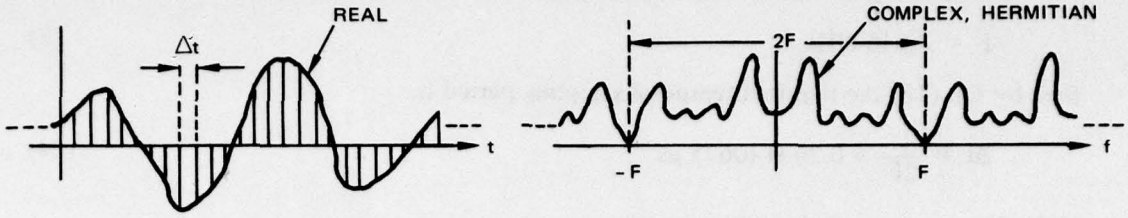
This results in a spectrum of bandwidth 2F (twice that obtained previously) but which is Hermitian. The temporal waveform therefore is real.



If this real temporal waveform is sampled at twice the highest frequency, that is, at intervals of Δt, where

$$\frac{1}{\Delta t} = 2F \quad (18)$$

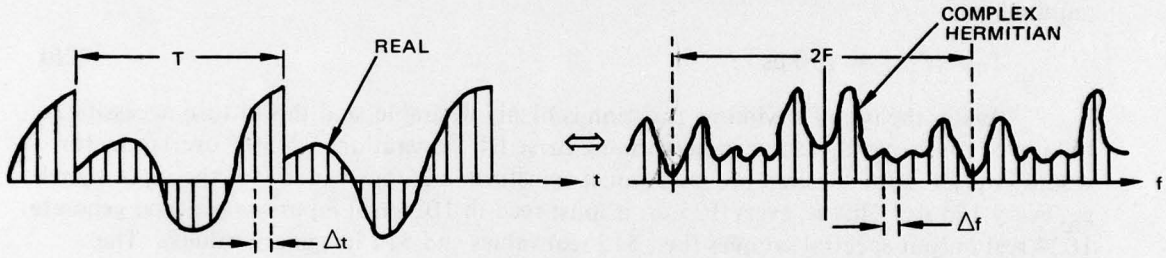
then the resulting spectral waveform is replicated about multiples of 2F.



Continuing as in the complex analysis, the spectral waveform must now be sampled at intervals of Δf Hz/sample. As before, this restricts the input waveform to an interval of T seconds, where

$$T = \frac{1}{\Delta f} \quad , \tag{19}$$

and replicates this waveform in time space about multiples of T seconds. That is,



The conservation of degrees of freedom argument is slightly more complicated in this analysis than before because of the need to consider complex variables as containing two real degrees of freedom. Clearly the number of real samples in the time-space window is

$$N'\,(\text{real}) = \frac{T}{\Delta t} \quad . \tag{20}$$

The number of real degrees of freedom in frequency space is twice the number of complex samples; thus

$$N\,(\text{complex}) = \frac{N'\,(\text{real})}{2} \quad . \tag{21}$$

However, the Hermitian constraint implies that only one-half of the $2F/\Delta f$ complex samples are independent; therefore

$$N\,(\text{complex}) = \frac{N'\,(\text{real})}{2} = \frac{1}{2}\left(\frac{2F}{\Delta f}\right) \quad . \tag{22}$$

Combining Eqs. (21) and (22) yields

$$N'\,(\text{real}) = \frac{T}{\Delta t} = \frac{2F}{\Delta f} \quad . \tag{23}$$

This differs from Eq. (5) by the factor of 2 anticipated by the conversion to real data from complex.

Proceeding as before, if the input signal bandwidth of interest is

$$F = 2.048 \text{ MHz} \tag{8}$$

then by Eq. (18) the required temporal sampling period is

$$\Delta t = \frac{1}{2F} = 0.244140625 \ \mu s \ . \tag{24}$$

If the frequency resolution of interest is

$$\Delta f = 4 \text{ kHz} \tag{10}$$

then by Eq. (23) the number of real samples to be utilized in the DFT operation is

$$N' \text{ (real)} = \frac{2F}{\Delta f} = \frac{4.096 \text{ MHz}}{0.004 \text{ MHz}} = 1024 \ . \tag{25}$$

Inserting these two results into Eq. (20) yields the total integration time (or window length) required as

$$T = N' \Delta t = 250 \ \mu s \ . \tag{26}$$

Again, the use of a window function is highly desirable, and this in turn necessitates the use of some overlap factor in performing these DFT operations. A 50% overlap factor would imply that the desired processor must transform a 250-μs window of the input signal, g_n, every 125 μs. That is, every 125 μs, it must read in 1024 real input samples and generate 1024 real output spectral samples (i.e., 512 real values and 512 imaginary values). The effective throughput rate is therefore

$$\frac{1024 \text{ real samples}}{125 \ \mu s} = 8.192 \text{ M } \frac{\text{real samples}}{\text{second}} \ . \tag{27}$$

As expected, the factor of 2 difference between Eqs. (13) and (27) is due to the use of real instead of complex input samples. The processing rate (in terms of real operations per second) is the same regardless of the mathematical notation.

With this analysis completed, a common notation has been developed to use in the following technology investigation.

3. FILTER-ARRAY SPECTRUM ANALYZERS

In seeking ways to implement the desired spectral decomposition, one may see advertised a large variety of "signal analyzers," such as the Hewlett Packard model 8565A, described in the next two pages. Such units perform a power spectrum analysis on incoming signals with frequency content of several MHz to several GHz. They are capable of achieving resolutions as fine as

$$\Delta f = 100 \text{ Hz.}$$

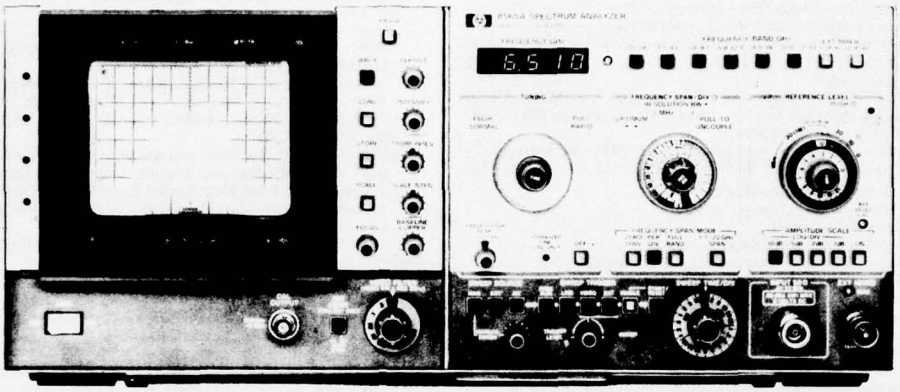
They are readily available, utilize existing low-risk technology, are compactly packaged, and are moderately priced. For example, the model advertised in the next two pages costs about $18,000.00, consumes 220 W, and occupies 7½ in. of rack space.

SIGNAL ANALYZERS

Spectrum Analyzer, 10 MHz to 40 GHz

Model 8565A

- 0.01 to 22 GHz coverage with internal mixer
- Internal preselection 1.7 to 22 GHz
- Wide choice of resolution bandwidths
- Simple three knob operation
- Absolute amplitude calibration
- CRT bezel readout displays control settings



8565A Spectrum Analyzer

Covering from 0.01 to 22 GHz with its internal mixer, the 8565A has built-in preselection and brings accuracy plus convenience to microwave spectrum analysis. The wide range, spurious-free display, compact design and ease of use make it well suited for lab, production, or field applications requiring accurate measurement from IF thru microwave frequencies. The 8565A can cover 0.01 to 22 GHz in just two spans for rapid location of signals prior to close-in analysis in one of six bands. Coverage is easily extended up to 40 GHz with the HP 11517A External Mixer.

High Resolution

Fully automatic stabilization in narrow spans reduces residual FM and drift. Standard resolution bandwidths range from 1 kHz to 3 MHz. The 1 and 3 MHz bandwidths allow fast sweeps in wide spans and increased dynamic range for pulsed RF; narrow bandwidths for measurement of closely spaced signals. Option 100 provides additional 100 Hz and 300 Hz IF bandwidth filters, and residual FM is <100 Hz when stabilized. This 100 Hz resolution is useable up to 8.5 GHz and the 300 Hz resolution bandwidth to 22 GHz. All resolution filters are gaussian-shaped for repeatable measurements, faster non-distorting sweeps and best pulse response.

Absolute Amplitude Calibration

Absolute signal levels from −112 dBm to +30 dBm are easily measured because the HP 8565A always displays the value of the reference line with LED's in the CRT bezel and at the reference level control. Changes in RF, IF gain, and preselector loss are automatically included. In addition, flat frequency response insures accuracy for relative as well as absolute power measurements.

Wide Dynamic Range

Internal preselection (1.7 to 22 GHz) enables you to measure distortion products as much as 100 dB down. Even for closely spaced signals or measurements below 1.7 GHz, all distortion products are greater than 70 dB down. In either case, maximum dynamic range is assured even for 1 watt signals with the 70 dB input attenuator. An input limiter (0.01 to 1.8 GHz) and the internal preselector (1.7 to 22 GHz) enable the 8565A to withstand RF signals up to +30 dBm for all input attenuator settings.

Designed For Convenience

Coupled controls allow you to make most measurements in 3 simple steps. Green color coded keys preset the 8565A for normal operation so a measurement only requires that you tune to a signal, select a desired span, and raise it to the reference level. Automatically selected sweep times insure a calibrated display for all combinations of frequency span, resolution bandwidth and video filtering.

The CRT bezel LED's display all pertinent control settings to give you all the information needed for signal evaluations in one central location. These data are also captured in CRT photos.

8444A Option H59 Tracking Generator

Make swept frequency response measurements to ± 1.7 dB from 10 to 1300 MHz (± 2.5dB up to 1500 MHz) with greater than 90 dB of dynamic range. The output is absolutely calibrated at 0 dBm and continuously variable to <−10 dBm . The frequency of unknown signals as well as the frequency of any point on the frequency response curve can be measured from the external counter output using the low-cost HP 5300/5305B Counter.

8750A Storage-Normalizer

The analyzer is made even easier to use with the digital storage of the 8750A because there is no need to re-adjust intensity or persistence as the sweep time changes. With the push of a button, a signal can be frozen on the CRT and then compared directly to the current input signal. Traces can also be compared arithmetically (i.e., normalized) to automatically remove frequency response variations. This is especially useful when used with the HP 8444A Opt. H59 Tracking Generator.

8565A Specifications

Frequency Specifications

Frequency range: 0.01 to 22 GHz with internal mixer, 14.5 to 40 GHz with HP 11517A External Mixer.

Tuning accuracy (digital frequency readout in any span mode)

Internal mixing: 0.01 to 2.5 GHz < ± 5 MHz, ± 20% of Freq. Span/Div; 2.5 to 22 GHz, ± 0.2%, ± 20% of Freq Span/Div.

External mixing: 14.5 to 40 GHz < ± 0.7%, ± 20% of Freq Span/-Div.

Frequency spans

1.7 to 22 GHz: multiband span from 1.7 to 22 GHz in one sweep.

Full band: displays spectrum of entire band selected.

Per division: eighteen calibrated spans from 1 kHz per div. to 500 MHz per div. in a 1, 2, 5 sequence, plus a full band span, "F".

Span width accuracy: the frequency error for any two points on the display for spans from 500 MHz/div to 20 kHz/div (unstabilized) is less than ± 5% of the indicated separation; for stabilized spans 100 kHz/div and less, the error is less than ± 15%.

Zero span: analyzer becomes a manually tuned receiver.

Spectral resolution and stability

Resolution bandwidths: resolution (3 dB) bandwidths from 1 kHz to 3 MHz in 1, 3, 10 sequence. Bandwidth and span width are independently variable or may be coupled for optimum display when control markers are aligned (▶◀).

Resolution bandwidth accuracy: 3 dB points: < ± 15%.

Selectivity (60 dB/3 dB bandwidth ratio): <15:1.

Stability: Total residual FM (fundamental mixing 0.01 to 4.1 GHz): stabilized, <200 Hz p-p in. 0.1 sec; unstabilized <10 kHz p-p in 0.1 sec.

Stabilization range: first LO automatically stabilized for frequency spans 100 kHz/div or less. First LO residual FM typically 30 Hz p-p when stabilized.

Noise sidebands: >70 dB down, >30 kHz from center of CW signal in a 1 kHz Res. Bandwidth and a 10 Hz (0.01) Video Filter.

Amplitude Specifications

Amplitude range – internal mixer

Measurement range

Total power: +30 dBm (1 watt).

Damage levels: (50Ω nominal source impedance.)

dc: 0 V with 0 dB input atten, ± 7 V with ≥10 dB input atten.

ac: 0 V with 0 dB input atten, 10 V peak with ≥10 dB input atten.

RF: (signals above 10 MHz) + 30 dBm for any attenuator setting.

Gain compression: <1 dB for 0 dBm input level with 0 dB attenuation.

Average noise level: max. avg. noise level with 1 kHz Res. Bandwidth (0 dB atten and 3 Hz video filter) is in the table below:

Frequency Band (GHz)	First IF in MHz	Harmonic Mode	Noise Level (dBm)	Frequency Response* (± dB MAX)
1.8	2050	1–	–112	1.2
1.7–4.1	321.4	1–	–109	1.7
3.8–8.5	321.4	2–	–103	2.5
5.8–12.9	321.4	3–	–94	2.5
8.5–18	321.4	4+	–87	3.0
10.5–22	321.4	5+	–75	4.5

*Frequency response includes input attenuator, preselector and mixer frequency response plus mixing mode gain variation (band to band).

Amplitude range - HP 11517A External Mixer

Measurement range : saturation (gain compression <1 dB), –15 dBm. Damage level >0 dBm or 0.1 erg.

Sensitivity (Average noise level in a 10 kHz IF bandwidth): 14.5–18 GHz <–80 dBm, 18–26.5 GHz <–70 dBm, 26.5–40 GHz <–60 dBm. Typical sensitivity is 10 dB better for each band.

Reference Level

Reference level range +70 dBm (+30 dBm max. input) to –102 dBm in 10 dB steps and continuous 0 to –12 dB calibrated vernier.

Reference level accuracy: the Auto Sweep setting of the sweep time/div control insures a calibrated display within these limits:

Calibrator output (100 MHz ± 10 kHz): –10 dBm ±0.3 dB.

Reference level variation (input attenuator at 0 dB): 10 dB steps < ±0.5 dB (0 to –70 dBm); < ±1.0 dB (0 to –90 dBm).

Vernier (0 to –12 dB) continuous: maximum error <0.5 dB.

Input attenuator: (at preselector input, 0-70 dB in 10 dB steps).

Step size variation: < ±1.0 dB, 0.01 to 18 GHz; < ±1.5 dB, 0.01 to 22 GHz.

Maximum cumulative error over the 0 to 70 dB range: < ±2.8 dB, 0.01 to 18 GHz; < ±4.0 dB, 0.01 to 22 GHz.

Frequency response: see table above.

Switching between bandwidths: 3 MHz to 1 kHz, ±1.0 dB

Calibrated display range

Log: (expanded from reference level down): 70 dB @ 10 dB/div, 40 dB @ 5 dB/div, 16 dB @ 2 dB/div and 8 dB @ 1 dB/div.

Linear: full scale from 1.8μ V (–102 dBm in 50 Ω to 707 volts (+70 dBm) in 10 dB steps and continuous 0 to –12 dB vernier.

Display accuracy

Log: < ±0.1 dB/dB, but < ±1.5 dB over full 70 dB display range.

Linear: < ±0.1 division over full 8 division deflection.

Residual responses (no signal present at input): with 0 dB input atten, fundamental mixing (0.01 to 4.1 GHz) <–90 dBm.

Signal identifier: available on all bands, used in 1 MHz/div span for signal identification

Signal Input Characteristics

Input 50Ω 0.01 to 22 GHz

Input connector: precision Type N female.

Input impedance

Input attenuator at 0 dB: 50 ohms nominal.

SWR: <1.5, 0.01 to 1.8 GHz; <2.0, 1.7 to 22 GHz (at analyzer tuned frequency).

Input attenuator at 10 dB or more: 50 ohms nominal.

SWR: <1.3, 0.01 to 1.8 GHz; <2.0, 1.7 to 22 GHz.

LO Emission (2.00 to 4.46 GHz): –50 dBm, 0.01 to 1.8 GHz; –85 dBm, 1.7 to 22 GHz.

Input protection (for input signals from 0.01 to 22 GHz)

0.01 to 1.8 GHz frequency band: internal diode limiter.

1.7 to 22 GHz frequency bands: saturation of YIG filter (preselector) occurs at total input signal power levels below input mixer damage.

External mixer input: BNC female connector is a port for LO power transfer, bias current and IF return.

Sweep Specifications

Sweep time

Auto: sweep time is automatically controlled by Frequency Span/-Div, Resolution Bandwidth and Video Filter controls to maintain an absolute amplitude calibrated display.

Calibrated sweep times: 21 internal sweep times from 2 μsec/div to 10 sec/div in 1, 2, 5, 10 sequence.

Display Characteristics

Cathode Ray Tube (aluminized P31 phosphor, 8 x 10 div internal graticule)

Persistence

Conventional: natural persistence of P31 phosphor.

Write: continuously adjustable from 0.2 sec to full storage.

Storage time: continuously adjustable from 1 minute (full brightness) to >30 minutes (minimum brightness).

CRT Bezel Readout: bezel LEDs display *the following measurement* data (included in CRT photographs taken with the HP 197A Opt 001, 006 Oscilloscope Camera): Ampl. Scale Factor, Ref. Level, Input Atten., Res. Bandwidth, Sweeptime/Div., Freq., Freq. Span/Div.

General Specifications

Temperature range: operating 0°C to 55°C, storage –40° to +75°C.

Humidity range (Operating): <95% R.H. 0°C to 40°C

EMI: conducted and radiated interference is within the requirements of methods CE03 and RE02 of MIL STD 461A, VDE 0871 and CISPR pub'n 1, 2 and 4.

Power requirements: 48-66 Hz, 100, 120, 200 or 240 volts (–10% to +5%) 220 V A max (400 Hz operation available as Opt 400).

Size: 188 H x 426 W x 552 mm D (7⅜" x 16¾" x 21¾").

Weight: net 29.1 kg (64 lbs). Shipping 38.6 kg (85 lbs).

Standard Options Available

Opt 100, 100 and 300 Hz Resolution Bandwidths: adds 100 Hz and 300 Hz resolution bandwidths with 11:1 shape factor, residual FM <100 Hz when stabilized and improves sensitivity by 10 dB.

Opt 200—Calibration in dBμV

Opt 400—400 Hz Power Supply

Ordering Information

8565A Spectrum Analyzer

Opt 100: 100 Hz and 300 Hz Resolution Bandwidths

Opt 200: Calibration in dBμV

Opt 400: Internal 50 to 400 Hz Power Supply

Opt 907: Front Handle Kit

Opt 908: Rack Flange Kit

Opt 909: Rack Flange and Front Handle Kit

Opt 910: Extra Operating and Service Manual

11517A External Mixer (taper section req'd)

11518A Taper Section, 12.4 to 18 GHz

11519A Taper Section, 18 to 26.5 GHz

11520A Taper Section, 26.5 to 40 GHz

8444A Opt H59 Tracking Generator, 10 to 1500 MHz

8750A Storage-Normalizer

The drawback to such units, at least for the application of interest, is that they compute only the power spectrum, not the complex amplitude of the frequency distribution. Hence the spectral decomposition cannot be used for complex demodulation as required herein.

4. DIGITAL ELECTRONICS

A. GENERAL-PURPOSE COMPUTERS

In a typical general-purpose (GP) computer of the classic Von Neuman architecture, input data is brought into an input buffer memory. A sequence of microprogram instructions then directs the arithmetic logic unit (ALU) to perform various arithmetic and/or logic operations on this data and store it back in memory. When the desired sequence of operations is complete, the data is read out. A software program to directly perform the multiplications and summations indicated by Eq. (6) can readily be written; thus the GP computer is a candidate to be considered.

The primary differences between digital computers and the special-purpose pipelined signal processing modules to be discussed shortly (e.g., SAW devices, CCD's, optical processors) are in versatility and speed. Digital electronic components can perform a large variety of operations, both arithmetic and logic, on input data. (Hence, the primary measure of performance is "operations per second.") This contrasts sharply with the analog technologies of interest, which can only perform specific operations, such as multiplications. As we shall see, however, the increased versatility of digital computers is offset by much lower speed.

The DFT algorithm is multiplication-intensive, and the operation of "multiplication" is one that requires considerable time (compared, say, to additions or shifts) in digital implementation. Hence, in assessing how well a digital electronic processor performs the DFT algorithm, it suffices generally, as a first approximation, to consider only the time involved in performing the required multiplications and ignoring the processing time required for the remaining operations.

A modern state-of-the-art minicomputer system can perform a firmware fixed-point multiply instruction in, typically, 5 μs. (For example, the current Hewlett-Packard F-series CPU performs this operation in 6 μs.) The direct computation of Eq. (6) requires N^2 complex multiplications or $(N')^2$ real multiplications. The discussion of Section 2B shows that for the parameters of interest, the window length is 1024 real samples and the required throughput rate is one 1024-point window every 125 μs. However, a simple calculation shows that a typical general-purpose computer requires about 5 s to perform the multiplications for each window, i.e.,

$$(1024)^2 \ \frac{\text{multiplications}}{\text{window}} \cdot \frac{5\ \mu\text{s}}{\text{multiplication}} \approx \frac{5\ \text{s}}{\text{window}} .$$

This is a factor of 40,000 too slow.

Since the limiting factor of digital electronic implementations for signal processing tends to be the restricted multiplication rate, it becomes prudent to seek alternative algorithms for calculating the Fourier coefficients [other than the DFT algorithm of Eq. (6)] that reduce the number of multiplications at the expense of increasing the number of some other operation, which, it is hoped, the digital electronics can handle quickly.

Fortunately, there exists such an algorithm called the Fast Fourier Transform (FFT), which allows the computation of the spectral values, G_m, in only $N' \log_2 N'$ real multiplications

instead of the $(N')^2$ real multiplications required by the direct implementation of Eq. (6). The price paid for the decreased number of multiplications is a complex iterative routing of data and intermediate results; but storing and retrieving numbers in random-access memory is a much quicker operation than multiplication, so the use of this algorithm is highly beneficial. An analysis of the FFT is beyond the scope of this report and is well described in Refs. 2, 3, and 5. Using the FFT algorithm, a GP computer with a 5-μs multiplication time would require 50 ms to perform the multiplications for each window, i.e.,

$$1024 \log_2 1024 \ \frac{\text{multiplications}}{\text{window}} \cdot \frac{5\ \mu\text{s}}{\text{multiplication}} \approx \frac{50\ \text{ms}}{\text{window}} \ .$$

This is still a factor of 400 too slow.

Thus software or firmware implementation of the spectral analysis operation on a GP computer is far too slow to meet the desired specifications.

B. ARRAY-TRANSFORM PROCESSORS

An array-transform processor is a peripheral unit to be interfaced with a GP computer. It is specifically designed to handle those operations involving large arrays of numbers. Most units incorporate a hardware multiplication chip; hence they are considerably faster at performing the FFT operation than the GP computer itself. However, they still retain some degree of flexibility, so that they can be software-programmed to perform other array-intensive and multiplication-intensive operations, such as matrix inversion and correlation operations.

As typical examples of the state-of-the-art, three commercially available array processors are the model AP-120B by Floating Point Systems Inc., the model 100 by Floating Point Systems Inc., and the model MAP-300 by CSP Inc. These units are described more fully in Refs. 6, 7, and 8, respectively. The only specifications of interest here are the multiplication times, which are 167 , 250, and 210 ns, respectively. Simple calculation shows that the fastest unit performs the multiplications for a 1024-point window of real input data in 1.7 ms, e.g.,

$$1024 \log_2 1024 \ \frac{\text{multiplications}}{\text{window}} \cdot \frac{167\ \text{ns}}{\text{multiplication}} \approx \frac{1.7\ \text{ms}}{\text{window}} \ .$$

(Actually, the AP-120B specifications sheet lists 2.7 ms as the time required for a 1024-point real FFT when the time required for all the other operations is included.) While this speed is a big improvement over the GP computer, it is still a factor of about 14 times too slow for real time performance of the task stated in Section 2.

The accuracy of these machines is very good due to the use of floating point arithmetic. The AP-120B carries 38 bits of accuracy (a 10-bit binary exponent and a 28-bit two's complement mantissa), while the MAP-300 uses 32-bit numbers (a sign bit, a 7-bit hexadecimal exponent, and a 24-bit hexadecimal mantissa).

The main shortcoming of array processors for the intended application, however, is not their speed but their large size, large power consumption, and high cost. For example, the AP-120B occupies 6.4 ft^3, consumes 1200 W, and costs approximately \$40K (depending on memory options). Additionally, since array processors cannot operate as stand-alone units, all of this is in addition to the size, power consumption, and cost of the host computer.

C. SPECIAL-PURPOSE DIGITAL ELECTRONICS

A third alternative in the digital electronics arena is to dispense with the flexibility and programmability of the GP computer and the array processor, and to design and fabricate a module customized to the FFT algorithm with the parameters of Section 2. With such a special-purpose system, one would be limited only by the speed of the basic multiplication operation. (This assumes that high-speed bipolar memory is used so that the memory-access time is not the critical factor.) Fortunately, TRW manufactures a line of very high-speed multiplication chips well suited to this application. Their model TDC 1008 J performs the multiply-accumulate operation on 8-bit inputs in 70 ns, and their model TDC 1010 J performs it on 16-bit inputs in 115 ns. Advertisements for these two products are shown on the next two pages for illustration.

One detail of the FFT algorithm which impacts the choice between these two chips is that round-off errors which build in the iterative procedure limit the output accuracy. A common rule-of-thumb is that one loses ½ bit of accuracy for each iteration. Thus a 512-point complex FFT, which requires $\log_2 512 = 9$ iterations through the FFT's butterfly loop loses 4½ bits of accuracy. If 8-bit multiplications are performed, the final answer will have only 8 – 4½ = 3½ bits of accuracy, which is far too low for most useful applications. Use of the 16-bit multiplication chip, on the other hand will leave 16 – 4½ = 11½ bits of accuracy. This is far more useful, so the following discussion will consider this chip.

Assume that four such chips are utilized and are configured to perform a complex butterfly operation. Then the time required to perform the multiply-accumulate operations for performing an FFT operation on a 512-point window of complex input samples is 0.53 ms, i.e.,

$$512 \log_2 512 \ \frac{\text{multiplications}}{\text{window}} \cdot \frac{115 \text{ ns}}{\text{multiplication}} \approx \frac{0.53 \text{ ms}}{\text{window}} .$$

This is only a factor of 4 slower than the 125 μs specified in Section 2A.

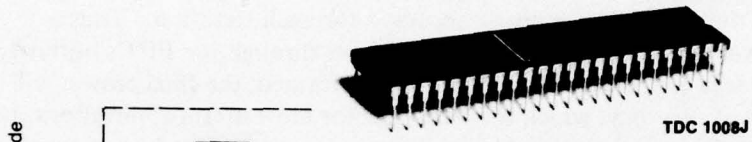
An estimate of the size and power requirements of such a system can be obtained from a preliminary circuit design for a stand-alone FFT module performed by Dr. Ed Wrench of NOSC. He calculated that a complete system would require about 75 chips for the processing subsystem and about 25 chips for the memory subsystem. These 100 chips would occupy two 5- by 9-in. circuit cards. The 4 multiplier chips would require 3½ W each; the 14 high-speed memory chips would draw ½ W each; and the remaining 82 chips would average about 1/10 W each. Thus the total power consumption would be about 30 W.

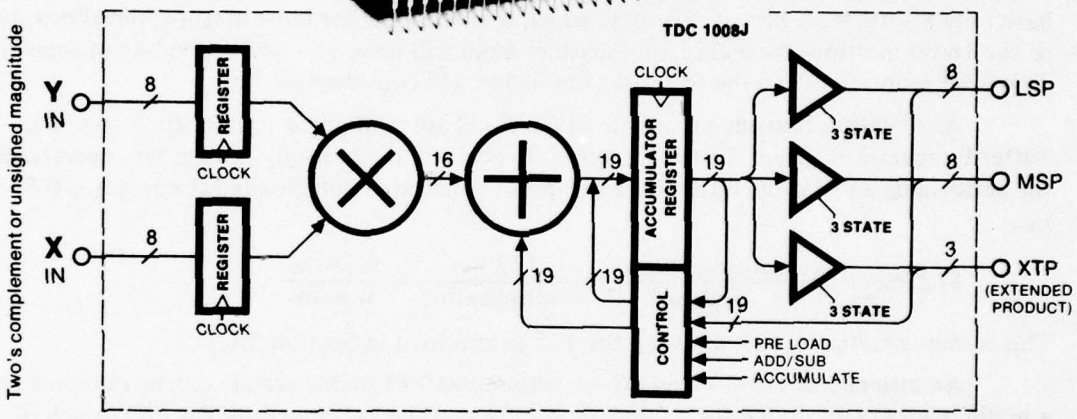
The speed, small size, moderate power requirements, and relatively good accuracy of this approach make it an attractive candidate for implementing the desired operation. Furthermore these parameters will rapidly get better due to (a) the considerable momentum of the commercial digital electronics field, and (b) the high throughput and high circuit density promised by DOD's Very High Speed Integrated Circuits (VHSIC) program in the signal processing area.

5. INCOHERENT OPTICAL PROCESSING

The chief advantages of optics for use in signal processing devices are (1) very high multiplication rates and (2) inherent parallelism due to the two-dimensional nature of light wavefronts. While most current research in the field emphasizes coherent optics (to be discussed in the next section), the use of noncoherent optics has much to offer. The price paid for

Wow! Now you can multiply...or multiply and accumulate in 70 nsec





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70 ns, 8 bits—$70 in 100's

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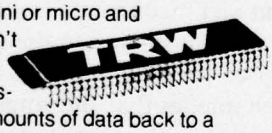
A small FFT processor based on TRW's new MAC operates as a spectrum analyzer too—add one to your mini or micro and you don't have to lug massive amounts of data back to a number-crunching mainframe for reduction; you can reduce it right there on site and in real time!



It can analyze voices, earthquakes, geological soundings and submarine signatures. It can recognize a sticky valve in an automobile engine or in a human heart.

There was a time when the phrase "FFT processor" conjured up the image of an entire bay of sophisticated electronic hardware, but that's all changed now.

Starting with just a single TDC 1010J, you can design your own FFT processor on a small pc card. It will operate on just a few Watts and the CPU's microcode need never even touch the data.

Simply strobe any pair of 16-bit numbers into the MAC's on-chip input registers and zip—the chip delivers the correct 32-bit product for you in a mere 115 nsec.

An on-chip, 35-bit wide accumulator lets you choose to sum a series of products with no time penalty; that's both a double-precision multiply and a 35-bit add in the same 115 nsec!

Flexibility is a key feature of the TDC 1010J—it works on numbers as either two's complement or unsigned magnitude; the 35-bit accumulator can be directly pre-loaded, and you can round off the accumulated products to single precision.

Our new MAC is fully compatible with industry standards TTL. (It should be—after all, TRW invented TTL and patented it back in the early '60's, remember?) Of course, 3-state output buffers are provided.

TRW's TDC 1010J multiplier/accumulator is packaged in a 64 pin DIP. It consumes just 3½ Watts, uses a single +5V supply and is radiation hard. It is priced at only $205 in quantities of 100.

Like all TRW LSI Products, the TDC 1010J multiplier/accumulator is available now from stock through Hamilton Avnet. For more information, send in the coupon or talk to one of our digital signal processing experts at 213/535-1831.

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relinquishing the separate control of amplitude and phase information obtainable in coherent systems is the necessity to process complex data as two real quantities. However, as discussed in Section 2B, this does not present any difficulty in this application. What one gains by utilizing incoherent light is the freedom from vibration problems, thermally produced aberrations, and costly high-quality optics characteristic of the coherent approach.

The two papers reprinted in Appendix A present a particular approach to incoherent optical processing, named the electro-optical processor (EOP), that seems well-suited to the problem at hand. The first paper (Ref. 9) discusses the theory, design, and application of such devices and ends by detailing plans for fabricating in FY 80 a CCD that would give an EOP an input rate capability of 1M samples/sec while performing a 128-point DFT operation.

The second paper (Ref. 10) gives technical details of presently existing EOP's capable of performing 512-point sliding-window DFT operations with input rates of 32K samples per second.

The strengths of this approach are:

- small size (2 $in.^3$ for the EOP module and one small circuit board for a complete DFT subsystem)
- low power (<5W)
- potentially low cost (ultimately <$1K for a 512-point 1M samples/sec DFT system)
- any desired window function can be incorporated on the CCD mask and processed with no extra components or processing time
- any set of frequencies can be calculated (e.g., logarithmically spaced frequencies, or only over a limited set of frequencies)
- useful for other signal processing operations, such as beamforming and correlation.

6. COHERENT OPTICS TECHNOLOGY

Since the advent of the laser in 1960 the field of coherent optical signal processing has attracted considerable attention. Excellent references to this technology are the text by Goodman (Ref. 11) and the review paper by Vander Lugt (Ref. 12). As mentioned in the last section, the two great strengths of the use of optics (both coherent and incoherent) in signal processing are (a) very high multiplication rates, and (b) inherent parallelism due to the two-dimensional nature of light wavefronts. In addition to these, the two peculiar strengths of *coherent* optics are (a) the complex nature of the light field, which implies that the amplitude and phase of a complex number can be propagated through the system as the amplitude and phase of the light wavefront at a given point, and (b) the speed-of-light calculation of the two-dimensional Fourier transform. In a coherent optical system the relationship between the complex amplitude light distributions in the front and back focal planes of a lens is that of a Fourier transform. In practice, the throughput of such systems is limited by the rate at which input data can modulate the light field in the front focal plane and, to a lesser degree, by the rate at which the output values can be detected and read out of the back focal plane. Two types of real-time input transducers of interest here are the two-dimensional spatial light modulators (SLM's) and the Bragg cell. These shall be discussed separately.

A. COHERENT OPTICAL PROCESSING WITH A TWO-DIMENSIONAL SLM

Since 1960 considerable effort has gone into the development of real-time two-dimensional SLM's to act as input transducers for coherent optical systems. The desired characteristics of such devices are:

- read, write, erase capability
- storage capability
- high frame speed
- high space-bandwidth product
- grey level capability (dynamic range)
- high uniformity
- long recycle lifetime
- environmental stability
- economically available.

Several candidate materials exist and are currently under development. These include

- ferroelectric ceramics
- liquid crystals
- magnetic bubble domains
- Pockel's effect crystals
- photodichroic crystals
- deformation devices
- membrane light modulators
- thermoplastics.

Reference 13 by Casasent reviews the strengths and weaknesses of most of these.

The number of real sample points per DFT window in the specifications of Section 2B is 1024, which approximately matches the number of resolution cells per scan line of these SLM's and matches the one-dimensional space-bandwidth product of good quality optics. So resolution is not a problem. Also the speed requirement is within the state-of-the-art. Most of these SLM's can operate at standard television rates, namely, 63.5 μs per scan line. If a scan line contains the 1024 real input samples then this technique is twice as fast as required for the desired task.

A problem with coherent optics is that it basically is not a good match for the application under discussion. Coherent optical processing systems with two-dimensional SLM's perform two-dimensional Fourier transforms, whereas the application requires only one dimension. True, by utilizing cylindrical optics the second dimension can be used to perform many one-dimensional transforms in parallel, but aspheric optics is both expensive and of inferior performance. Also, by raster-scanning the input and output planes, the second dimension can be utilized to transform a very long input signal, but the 1024 real points per window of interest here hardly falls into that category.

A more serious problem with this approach is that most real-time two-dimensional SLM systems are bulky, expensive, and not ruggedized. The electron-beam addressed systems require high voltages, and the laser-beam addressed units require registration and alignment. Major breakthroughs are required before such devices become practical (i.e., rugged, reliable, small size, low cost, low power) for field usage.

B. ACOUSTO-OPTICAL PROCESSING USING A BRAGG CELL

As depicted in Fig. 1, a Bragg cell is a device for converting an input voltage waveform into a bulk acoustic wave propagating through a crystal material that, in turn, modulates the phase of a coherent beam of light passing through it. It is a very useful and well-developed method for inputting one-dimensional real-valued serial data into a coherent optical system. The Applied Technology Divison of ITEK Corporation has developed several such systems for

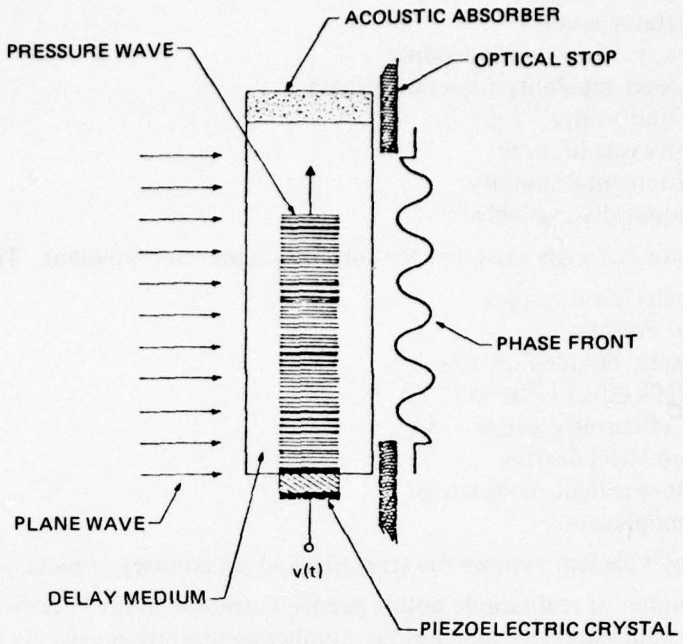


Figure 1. Acoustic light modulator.

ECM and radar signal analysis (Ref. 14). References 15 and 16 overview some recent work in the field. These units operate with center frequencies of 50 MHz to over 1 GHz and with bandwidths of from a few MHz to over a GHz. Thus the total bandwidth is more than required for the parameters of interest. Also the 1000-spot time-bandwidth product matches nicely with the 1024-point windows of real input data required. The problem is in the area of integration time. Section 2B requires a total integration time of 250 μs in order to achieve the desired 4 kHz resolution. Since the acoustic velocity in lithium niobate is 6.5 mm/μs, a Bragg cell of 1.6 m in length would be required. Clearly this is impractical. Even if such a single crystal could be grown, the acoustic attenuation from one end to the other would be a problem, and the resultant system would be very bulky.

C. COHERENT DETECTION

As mentioned earlier, the amplitude and phase of the light field in the back focal plane of the lens is the Fourier transform of the input; however, detecting this complex light field is a non-trivial problem. The usual system simply detects the *intensity* (i.e., the squared modulus of the complex light values) and acts therefore as a power spectrum analyzer. Reference 17 discusses techniques in which a reference light beam, coherent with the first, is used to also illuminate the output plane. The intensity of the resultant interference pattern then yields the required amplitude and phase information. Unfortunately, optical interferometers are notoriously unstable, hence, extreme precautions must be taken against vibration, air currents, and thermal degradation.

7. FIBER OPTIC COMB FILTER

Another signal processing technology of interest here is the use of fiber optics to form a transversal filter. The basic concepts, as reported by Taylor, Dillard, and Hunt (Refs. 18, 19) are shown in Fig. 2.

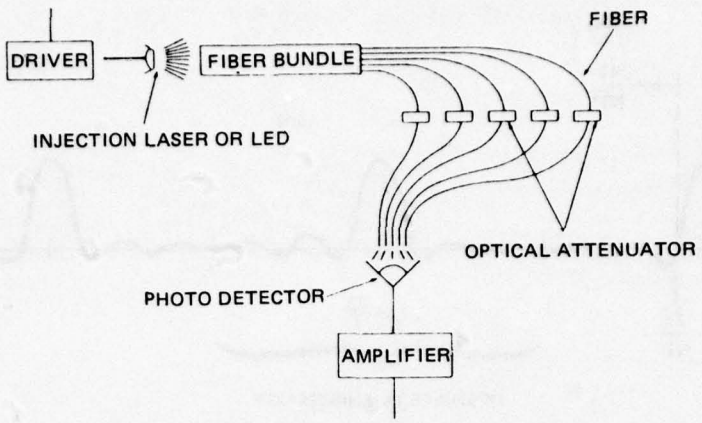
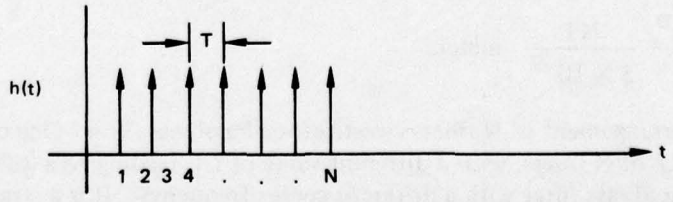


Figure 2. The fiber optic transveral filter.

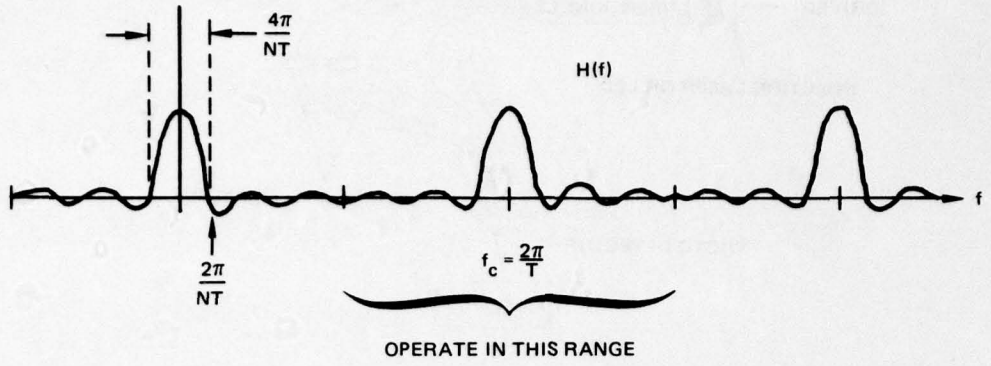
The input signal, g(t), temporally modulates the optical output of the light source, typically an injection laser or a light-emitting diode (LED). (Since the intensity out of an LED is linearly related to the current in, this technique is capable of processing analog data.) This light is then coupled into a bundle of N optical fibers each having a different length, L_n, where n = 1, 2, 3, - - -, N. Thus, each fiber introduces a different delay time $T_n = v\ L_n$, where v is the velocity of light in the fiber. As shown in the figure, each fiber can also be coupled through an optical attenuator in order to modulate the intensity transmittance of each fiber, although this feature will not be utilized here. The output of the fiber bundle is then detected by a single photodetector where a summation (i.e., energy integration) of the outputs of the N fibers takes place. It can be shown that this is a linear system, where the output is simply the convolution of the input signal with an impulse response defined by the time delays and attenuation factors of each fiber. In other words, this implementation forms a finite impulse response (FIR) filter or a transversal filter.

If each fiber delays the signal by some amount T_n between the source and the detector (i.e., no attenuation), and if the length of each fiber is an integral multiple of the length of the shortest one (i.e., the n^{th} fiber has length nL_1), then the impulse response of the system is the well-known comb function, consisting of N equally spaced impulses, i.e.,

$$h(t) = \sum_{n=1}^{N} \delta\,(t - nT) \tag{28}$$



As discussed earlier, convolution in time space is equivalent to multiplication in frequency space by the Fourier transform of h(t). The Fourier transform of a sequence of N equally spaced impulses is a series of sinc functions of mainlobe width $4\pi/NT$ and center-to-center spacing $2\pi/T$, i.e.,



If we restrict the input signal to contain only frequencies between π/T and $3\pi/T$, then this "comb filter" acts like a bandpass filter whose

$$\text{center frequency} \equiv f_c = \frac{2\pi}{T} \tag{29}$$

and whose

$$\text{bandwidth} \equiv BW = \frac{2\pi}{NT} \quad . \tag{30}$$

It shall be mentioned in passing without further elaboration that by introducing an attenuation capability into each fiber, one can "shape" the impulse response to obtain filter envelopes with lower sidelobe levels than the sinc function.

The velocity of light in fibers is nominally

$$v = \frac{5\ \mu s}{km} \quad . \tag{31}$$

Thus the length of the shortest fiber, the one producing a delay of T seconds, is given by

$$L_1 = \frac{T}{5 \times 10^{-9}} \text{ meters,} \tag{32}$$

and the length of the longest fiber, the one producing a delay of NT seconds, is

$$L_N = \frac{NT}{5 \times 10^{-9}} \text{ meters.} \tag{33}$$

Thus, this arrangement of N fibers constitutes a bandpass filter. One can easily imagine a second group of N fibers, with a different value of L_1, leading to a different photodetector to form a bandpass filter with a different center frequency. It is a straightforward extension of this principle to construct an array of M bandpass filters with each of the M sets of N fibers having a different value of L_1. If the center frequencies are at integer multiples of $2\pi/NT$ across the range of π/T to $3\pi/T$ Hz, then one has in essence a spectrum analyzer with M = N frequency bins. The system requires one LED, N^2 fibers, and N photodetectors.

Let us now consider two cases. The first case assumes that the signal z(t) as detected at the receiver is used to modulate the light source without first hederodyning it to baseband. If f_c is 10^9 Hz, then

$$T = \frac{2\pi}{f_c} = \frac{2\pi}{10^9} \text{ seconds.} \tag{34}$$

If the desired bandwidth is BW = 4×10^3 Hz as prescribed in Section 2, then

$$N = \frac{2\pi}{(BW)T} = \frac{2\pi}{(4 \times 10^3)\left(\frac{2\pi}{10^9}\right)} = 250{,}000. \tag{35}$$

For the filtering channel centered at $f_c = 2\pi/T$ Hz, the shortest fiber would have length

$$L_1 = \frac{T}{5 \times 10^{-9}} = \frac{2\pi}{5 \times 10^{-9} \times 10^9} = 1.25 \text{ meters} \tag{36}$$

and the $250{,}000^{th}$ fiber would have length

$$L_{250,000} = NL_1 = 314.159 \text{ km.} \tag{37}$$

Clearly such a large number of fibers ($N^2 = 6.25 \times 10^{10}$) of such long lengths (up to 314 km) is impractical.

Case number two assumes that the received signal is heterodyned down to a center frequency of 2 MHz before being inserted into this transversal filter. If f_c is 2×10^6 Hz, then

$$T = \frac{2\pi}{f_c} = \frac{2\pi}{2 \times 10^6} \text{ seconds.} \tag{38}$$

If the desired bandwidth is still 4 kHz, then

$$N = \frac{2\pi}{(BW)T} = \frac{2\pi}{(4 \times 10^3)\left(\frac{2\pi}{2 \times 10^6}\right)} = 500. \tag{39}$$

(f_c was chosen in order to make N, the number of frequency bins observable, come out to approximately 512 as desired for the parameters of Section 2.) For the filtering channel centered at $f_c = 2\pi/T$ Hz, the shortest fiber would have length

$$L_1 = \frac{T}{5 \times 10^{-9}} = \frac{2\pi}{(2 \times 10^6)(5 \times 10^{-9})} = 628 \text{ meters} \tag{40}$$

and the 500^{th} fiber would have length

$$L_{500} = NL_1 = 314 \text{ km.} \tag{41}$$

Thus, for a spectrum analyzer system to meet the specifications desired, one would require $N^2 = 250{,}000$ fibers ranging in length up to 314 km. It is the author's opinion that while such a unit could be fabricated for laboratory testing, major breakthroughs in the art of fiber bundle packaging are required to make such an implementation size and cost effective.

While this sytem has been discussed in terms of power spectrum analysis, it can be extended to perform a complex Fourier transform either by (a) using four such units in parallel (two each for the in-phase and quadrature inputs) with the impulse response of each group of N fibers tailored to be sine or cosine waveforms of various frequencies, or (b) using phase and amplitude modulation of a carrier as the input and complex detection to remove the effects of the carrier at the output. Such modifications obviously add to system complexity.

8. IMPLEMENTATIONS OF THE CHIRP-Z TRANSFORM

Equation (6) is the traditional form of the discrete Fourier transform equation. However, if the following substitution is made:

$$e^{-2mn} = \exp\left[m^2 - (n+m)^2 + n^2\right] , \tag{42}$$

one arrives at an alternative form of the Fourier transform known as the chirp-Z transform, CZT, (Ref. 3), namely

$$G_m = \exp\left(i\pi \frac{m^2}{N}\right) \sum_{n=1}^{N} f_n \exp\left(i\pi \frac{n^2}{N}\right) \exp\left[-i\pi \frac{(n+m)^2}{N}\right] . \tag{43}$$

This suggests the following algorithm for performing the Fourier transform operation:

1. Multiply f_n by the chirp waveform $\exp\left(i\pi \frac{n^2}{N}\right)$
2. Cross-correlate this result with the chirp waveform $\exp\left(-i\pi \frac{n^2}{N}\right)$ for a number of shifts m, and
3. Multiply this result by the chirp waveform $\exp\left(i\pi \frac{m^2}{N}\right)$.

The resulting coefficients G_m obtained from the CZT algorithm are identical to those obtained using the traditional algorithm of Eq. (6) even though quite a different mathematical procedure is used.

The use of this algorithm can be very beneficial if used in conjunction with hardware that performs the cross-correlation operation at very rapid rates. Two such hardware implementations are (a) surface acoustic wave (SAW) devices, and (b) charge-coupled devices (CCD's).

A. SURFACE ACOUSTIC WAVE DEVICES

SAW devices represent a very attractive implementation for the cross-correlation portion of the CZT operation. References 20 and 21 give more information than can be presented here. These devices work with either analog or sampled analog inputs and outputs. A typical device consists of a substrate of piezoelectric material on one face of which is deposited, by photolithographic techniques, a pattern of aluminum or other conductor electrodes. In its simplest configuration, these sets of interdigitated finger electrodes are spaced at the sampling rate distance through the use of the relationship $d_s = C_R t_s$, where d_s is the tap spacing, C_R is the Rayleigh wave velocity, and t_s is the sampling increment. For a typical substrate of ST-cut quartz, $C_R \approx 3$ mm/μs. Thus for an integration time of 250 μs (necessary to provide a resolution of 4 kHz), a quartz crystal of length 0.75 m would be required. This is far beyond the current capability (i.e., several inches); hence SAW technology is not a good

candidate to meet the specifications of Section 2. For applications requiring sampling rates of from 10 to 100 MHz, with carrier frequencies of from 50 to 500 MHz, and with typical fractional bandwidths of about 10% (i.e., 5 to 50 MHz), SAW transversal filters for implementation of the CZT hold great promise for low-cost, small-size, low-power systems.

B. CHARGE COUPLED DEVICES

A second technology worth considering for implementation of the cross-correlation portion of the CZT algorithm is charge coupled devices (CCD's). In fact, the advertisement copied on the following page shows a commercially available CCD chip designed for just that purpose. References 22, 23, and 24 give more information than can be presented here.

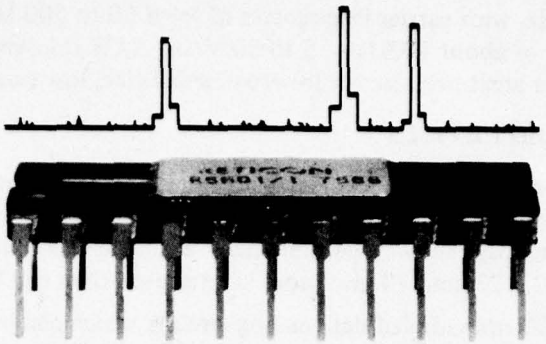
Basically, CCD's are sampled data analog circuits which can be fabricated by metal oxide semiconductor (MOS) technology as LSI components. As such they are directly compatible with other MOS circuits. State-of-the-art CCD transversal filters have operated as video devices with sample rates up to 10 MHz. CCD's operate by the manipulation of injected minority carriers in potential wells under MOS capacitors and thus behave as capacitive reactances with low power dissipation. However, the potential wells that contain the minority carriers also attract thermally generated minority carriers; hence there is a maximum storage time for the analog signals that depends on the dark current associated with the temperature of the silicon. At room temperature, storage times of hundreds of milliseconds are typical. Several different techniques are used to achieve unidirectional charge transfer. The first developed was a three-phase clocking structure in which the direction of charge propagation is determined by the sequence of potentials applied to the three electrodes.

In the so-called surface channel CCD's, if the minority carriers are allowed to collect at the semiconductor-oxide boundary, poor charge transfer efficiency will result due to minority carriers getting caught in trapping sites. This means that the CCD will behave nonlinearly unless there is sufficient propagating charge present to fill all of the traps. By biasing the operating condition of the CCD so that about 10% of the dynamic range is used for the injection of a "fat zero" bias charge, the traps are kept continuously filled and the device has over a 60 dB dynamic range. In practice, the input signal to be processed is added to a fixed bias somewhat larger than one-half of the peak-to-peak value of the signal before it is inserted into the CCD.

In general, CCD's have throughput rates of from 10 kHz to 10 MHz. For a 500-point line-array CCD, this translates to an integration time window of from 50 ms to 50 μs, which, for a Fourier transform operation, translates to frequency bin resolutions of 20 Hz to 20 kHz. These throughput rate and resolution figures indicate that CCD technology is a good candidate for meeting the desired specifications.

So far, we have only discussed the cross-correlation portion of the CZT algorithm, with the result that CCD technology shows considerable promise. We have yet to discuss the pre- and post-multiplication portions of the CZT operation and the generation of the required chirps waveforms. One approach to these tasks is to use off-the-shelf digital electronic technology, namely:

1. Perform an A/D conversion on the incoming signal.
2. Generate digital versions of the chirp waveforms by reading out high-speed ROM's.
3. Use the aforementioned TRW high-speed multiplication chip.
4. Perform a D/A conversion to obtain an analog signal to insert into the CCD cross-correlator.



The spectrum analyzer on a chip.

Where else but from Reticon.

What was previously thought impossible will now be an everyday occurence. Moving up to the next stage of complexity in CCD devices has resulted in the Reticon R5601, a 512 point Discrete Fourier Transformer. This technology offers a spectrum analyzer with small size, light weight, low power, high reliability, and a remarkable low cost. Along with its associated circuitry, it performs the Chirp Z algorithm to give a 256 spectral line display in less than 250 μsec. It's small enough to fit into your system, yet powerful enough to have a signal-to-noise ratio in excess of 70db. The numerous applications possible include speech recognition, target identification, vibration analysis, bandwidth compression, communications, and general signal analysis.

Currently available is a self-contained evaluation module on two printed circuit cards just 80 square inches. Just hook up your ±20 volts, display and you're on the air. Use the on-board oscillator or externally control the sampling rate.

The R5601 is the latest in our growing family of discrete time analog signal processing devices. All available through our worldwide network of over 20 distributors and more than 70 salesmen.

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5. Perform an A/D conversion.
6. Repeat steps 2 and 3 for the post-multiplication operation.
7. Perform a D/A conversion to provide an analog output for display.

This approach would consume too much power to really be cost-effective. An alternative approach, which eliminates the A/D and D/A converters, is the use of multiplying DAC's, wherein a digital signal (i.e., the chirp waveforms from ROM) controls the gain of the analog input signal. Unfortunately state-of-the-art multiplying DAC's have maximum throughput rates of a few hundred kHz, which is slower than the 8M samples/second rate specified in Section 2.

The use of analog technologies to perform these operations in a cost-effective manner appears promising. Texas Instruments has demonstrated a 32-point CZT device with the chirp-generators, multipliers, and CCD cross-correlator all on the same silicon chip. An alternate approach would be the development of high-speed switch-capacitor multiplying D/A converter chips, and the generation of analog chirp waveforms by pulsing a CCD transversal filter.

The CCD CZT approach has promise and appears a fruitful area for further development. Let us now look at what is commercially available today.

Reticon Corp. (Sunnyvale, CA) currently sells a single circuit board CZT device employing a CCD convolver chip for about $1600. It performs only a 256-point power spectrum, has a throughput rate of only 100 kHz, a dynamic range of 70 dB, an accuracy of only 8%, and computes each frequency from a different sliding window of the input data. Thus, their present device does not meet the specifications of Section 2.

This circuit board could be straightforwardly modified to perform a 512-point Fourier transform (i.e., real and imaginary inputs and outputs) in addition to performing the power spectrum, have a throughput rate of 200 kHz, and an accuracy of 1%. The speed is limited by the analog circuitry for the pre- and post-multiplications. The throughput rate could be increased to 2 MHz by employing digital circuitry at the expense of increased power consumption and circuit complexity, as discussed earlier. Also, the sliding-window feature could be circumvented by employing a recirculating delay line in the input at the price of halving the throughput rate or halving the number of points in the transform. Alternatively, the throughput rate could be increased by the development of high-speed analog multiplying chips so that a throughput rate of about 1 MHz could be achieved without the power and expense of digital external circuitry.

9. CONCLUSIONS

No technology meets the specifications of Section 2 with its present day state-of-the-art. Both the electro-optical processor (EOP) technology (performing a DFT or FIR filter bank) and the electronic CCD technology (performing a CZT) have high potential for doing so with some further development. The EOP requires the development of a 512 by 512 resolution-cell CCD with a shift-register rate of 4 MHz. Four such devices would then be required to meet the specifications of Section 2. Such developments are currently in progress at the Naval Ocean Systems Center and at RCA Laboratories (David Sarnoff Research Center) funded by the Naval Electronics Systems Command (NAVELEX). The electronic CCD CZT processor requires the development of high-speed analog multiplier technology (either on or off the CCD convolver chip). These efforts are currently being pursued at both Reticon and Texas Instruments. Due to the promising outlook offered by the electro-optical processor and electronic CCD technologies, more information on them is provided in Appendices A and B, respectively.

Digital FFT circuits employing TRW's high-speed A/D converter and multiplier chips meet the small-size and low-cost requirements and come within a factor of 4 of the speed specification but are power consumptive (say 30 W compared to just a few watts for the EOP and CCD devices). It is anticipated that increased speed and decreased power consumption should be achieved in the near future due to the considerable momentum of the commercial digital electronics field and the advances predicted by DOD's VHSIC program.

The remaining technologies are clearly inadequate, i.e., a major technology breakthrough would be required to cost-effectively meet the desired specifications.

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APPENDIX A

I. "An Electro-Optical Signal Processing Module"

II. "The EOP – A CCD-based Electro-Optical Processor"

AN ELECTRO-OPTICAL SIGNAL PROCESSING MODULE*

by

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Introduction

The authors have developed a new electro-optical signal processing module, just a few cubic inches in size, capable of performing a broad variety of general linear filtering operations at very rapid rates – typically greater than 10^9 multiplications per second. The distinct feature of this processor is its use of incoherent optics to achieve speed and parallelism in its operation. References 1–6 describe previous work in this technology. The present paper reviews the characteristics of this processing technique, describes the mathematical operations it is capable of performing, gives the operating parameters of the current implementation, and presents plans for modifications to even further improve its performance.

Processor Description

A mathematically rigorous treatment of the concept underlying the processor under discussion is contained in references 4 and 5; however, for overview purposes, the following qualitative description will be presented here. The processor, illustrated in Figure 1, consists of three components: a light-emitting diode (LED) illuminating a photographic transparency (or matrix mask) which in turn is in contact with an area-array charge-coupled device (CCD). Let the input signal be an analog sampled-data sequence, denoted by f_{n_o+n} with a sample rate of v_{in} samples/sec. Here, n_o is used to denote an arbitrary discrete time origin. This signal is used to temporally modulate the optical output of the LED. Thus the irradiance illuminating the photographic transparency is directly proportional to the input signal f_{n_o+n} and is spatially uniform across the entire surface of the mask. The transparency contains an M by K array of elements with optical transmittance values $h_{m,k}$ arranged in a geometrical pattern and scale identical to that of the photosite array in the CCD.* Since the irradiance transmitted by a transparency is the product of the illuminating irradiance times the intensity transmittance of the mask, the light distribution immediately behind the m,kth element of the transparency at the time when the n_o+n^{th} input sample is modulating the LED is proportional to $f_{n_o+n}\, h_{m,k}$. Assuming that the mask and the optically sensitive area of the CCD are in physical contact and registered such that the m,kth cell of the transparency is superimposed on the m,kth element of the CCD, then this irradiance pattern is detected by the CCD and stored as an M by K array of analog charge packets.

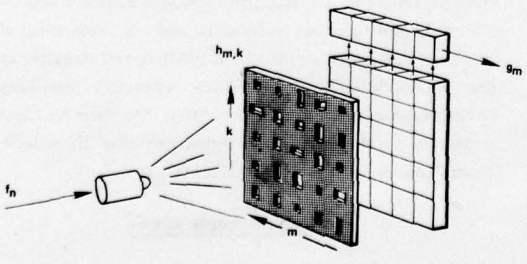

Figure 1. Basic components of the electro-optical signal processor.

By the nature of charge transfer technology, the application of clocking waveforms to the CCD electrode structure causes potential wells to "move" in such a way that these charge packets are shifted along the CCD structure (upward in the orientation of Figure 1). While the exact nature of these waveforms varies from manufacturer to manufacturer and from one model to the next, let us assume that the appropriate clocking pulses are provided so as to shift these charge packets vertically at a rate of v_{ver} CCD cells/sec. Let us further stipulate that $v_{ver} = v_{in}$, i.e., that the vertical shift rate (in CCD cells/sec) is the same as the input signal sample rate (in samples/sec). As these charge packets travel upward, more and more charge is added to them due to the time-varying pattern illuminating the CCD.** The net result is that each column of the CCD performs a running sum of the products of the time-varying LED radiance and the space-varying transmittance values of that column of the mask. In

*The intensity transmittance of the m,kth cell of the photographic transparency is proportional to the m,kth element of the matrix $[h_{m,k}]$. This can be achieved either by spatially modulating the grey scale of the film (which requires precise control of the photographic exposure and development processes) or by varying the area of transparent apertures in an otherwise opaque background (e.g., spatial pulse-width modulation). For experimental ease, the authors chose the latter approach.

**This mode of operation of the CCD is designated the "shift and add" mode or "time delay and integration (TDI)" mode, or even more simply, the "processing" mode to differentiate it from the more traditional imaging mode.

*Published in the Digest of Papers,
Government Microcircuit Applications Conference
Monterey, CA, 14-16 November, 1978

particular, let us consider the $k=n^{th}$ row of these charge packets. As this row travels from bottom ($k=n=1$) to top ($k=n=K$), its charge values take on the form

$$\sum_{n=1}^{K} f_{n_o+n}\, h_{m,n} \equiv g_{m,n_o} \qquad (1)$$

$$m = 1,2,3,\cdots,M$$

$$n_o = \cdots,-2,-1,0,1,2,\cdots .$$

where the unimportant constant of proportionality has been ignored for simplicity. Performing the operation of Eq. (1) in a fast, efficient manner is the major accomplishment of the electro-optical processor. We shall show shortly that this equation is the basis of many mathematical operations frequently used in a variety of signal processing applications.

The CCD chip contains a parallel-to-serial converter (physically just a horizontal linear CCD shift register with M input taps) and an on-chip amplifier so that this M-element vector can be read out of the CCD chip as a time-varying analog voltage waveform. It is important that the shift rate, v_{hor}, of this horizontal shift register be at least M times the shift rate of the vertical CCD registers in order that it be empty by the time the next row of charge packets, namely g_{m,n_o+1}, are ready to be read out. Thus, for the processing mode of CCD operation,

$$v_{in} = v_{ver} \leq \frac{v_{hor}}{M} \quad . \qquad (2)$$

This relationship between v_{ver} and v_{hor}, and relatedly the need for including the arbitrary time origin n_o in Eq. (1), are of fundamental importance in understanding the operation and capabilities of this processor. Figure 2 is a timing diagram showing the relationship between the input samples to the LED, f_{n_o+n}, and the output values, g_{m,n_o}, from the CCD's horizontal shift register. Note that this example depicts the most time-efficient case in which exactly M horizontal shifts occur between every vertical shift (and consequently between every input sample). Thus the inequality in Eq. (2) is an equality. This states that M samples come out of the CCD for each input sample going into the LED.

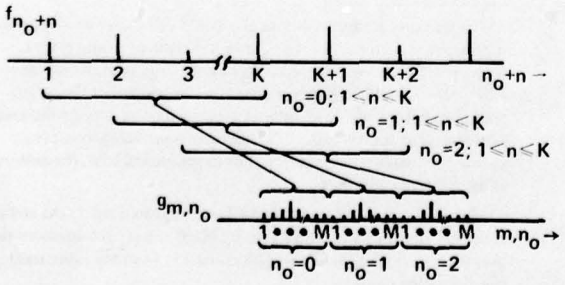

Figure 2. Timing relationship between input to LED and output from CCD for the case of sliding-window transformations. Overlap factor = (K – 1)/K

With reference to Figure 2, the relationship between these two time series is as follows: Assume that the processor is turned on at some arbitrary discrete time origin $n_o = 0$. While the first K input-signal samples are sequentially modulating the LED and the CCD vertical registers are shifting upward K times, the CCD horizontal register is spewing out (K – 1)M "garbage" values. Immediately after the K^{th} input-signal sample, the M values, $g_{m,0}$, outputted by the CCD horizontal register are valid data – constituting the M sums-of-products of the input sequence f_1 to f_K and the M columns of the mask $h_{m,k}$. Immediately after the $K+1^{st}$ input-signal sample modulates the LED, the M values, $g_{m,1}$, outputted by the CCD horizontal register again are valid data – constituting the M sums-of-products of the input sequence f_2 to f_{K+1} and the M columns of the mask. And so on. There are no more "garbage" terms after the initial start-up transient. Each sequence of M values from the CCD horizontal register is the sum-of-products of the previous K samples of the input signal with the M signals comprising the M columns of the mask. Thus every possible window of the input signal, f_{n_o+n}, $1 \leq n \leq K$, is multiplied and summed with the M reference signals on the mask. In other words the device simultaneously generates the M cross-correlation *functions* (e.g., the cross-correlation value for all values of time delay) between the input signal and the M reference signals on the mask.

An indication of the power of this module is that it contains the equivalent of (1) an M by K word ROM memory, namely the matrix mask, (2) a bank of M by K analog multipliers, (3) a bank of M by K analog adders, (4) a bank of M by K analog storage cells to store the cumulative sums, and (5) a parallel-to-serial converter to format these M parallel data streams into a single sequential output – all in the space of just a few cubic inches.

A restriction which the use of incoherent optics places on this processor is that, since light intensity and intensity transmittance can only be positive (i.e., non-negative) quantities, the input sequence f_{n_o+n} and the reference matrix $h_{m,n}$ must be positive quantities. However, this is not unduly restrictive since bipolar quantities can still be processed by either (1) adding a bias to them to make them non-negative, or (2) separating them into their positive and negative components and handling each of these separately. Similarly complex quantities must be separated into their real and imaginary parts. More detailed discussions of these techniques can be found in References 6 and 7.

Typical Applications

Multi-channel Cross-Correlation

As previously mentioned the electro-optical processor can be used to compute the cross-correlation functions between the input waveform f_{n_o+n} and the M signals $h_{m,n}$ comprising the M columns of the mask *simultaneously*. That is, it compares all time shifts, n_o, of the incoming signal with a

library of M reference signals in parallel. Such a multi-channel cross-correlation operation is very useful, for example, in an active radar system where the M reference signals might be dopplerized versions of the transmitted waveform, the input to the LED might be the received waveform, and thus the locations m, n_o of peaks in the CCD output would yield the range (proportional to n_o) and velocity (proportional to m) of any targets. Also, such a processor is useful in a non-synchronized communications receiver in which all time shifts of the incoming signal need to be cross-correlated with all members of a library of possible codewords.

Multi-channel FIR Filtering

For any given value of m, Eq. (1) defines the operation of a shift-invariant finite impulse response (FIR) filter.[8] Thus the electro-optical processor can be used as a multi-channel FIR filter; that is, each of the M columns of the mask can be a different FIR filter impulse response. Each column of the processor could then be, for example, a low-pass, high-pass, or band-pass filter with each column having a different cut-off frequency, bandwidth, or center frequency, etc.

General Linear Transformation

For any given value of n_o, Eq. (1) also defines the operation of a general linear filter, i.e., a "black box" characterized by an impulse response $h_{m,n}$. This filter or transformer need not necessarily be shift-invariant, for which the impulse response would reduce to h_{m-n}, and is therefore able to treat a larger class of useful linear transformations. The following list gives a few examples of useful signal processing transformations which can be performed by the electro-optical processor together with the appropriate form of the required matrix mask $h_{m,n}$:

Transform	Impulse Response
Convolution	h_{m-n}
Cross-correlation	h_{n-m}
Autocorrelation	f_{n-m}
Cosine transform	$\cos(2\pi mn)$
Fourier transform	$\exp(-2\pi imn)$
Laplace transform	$\exp(-mn)$
Hankel transform	$2\pi J_o(2\pi mn)n$

Putting this in another way, the processor is a linear system whose impulse response is determined solely by the optical transparency placed on the CCD. References 4, 5 and 6 show some typical masks for performing cosine, Fourier, and Hadamard-Walsh transforms.

Reference to Eq. (1) shows that the electro-optical processor performs these transforms on the input signal for every consecutive value of n_o. In other words, it performs a sliding-window transform; it performs the matrix-vector multiplication operation of Eq. (1) on every K-point window of the input signal. This feature is critically important in those applications where the time of arrival of the incoming signal is unknown, and hence transformations must be performed for all possible arrival times (or at least with a high degree of window overlap). A modification to the CCD architecture which would allow transformations with any arbitrary degree of window overlap, and a consequent increase in input data rate, will be discussed shortly.

A final comment on this implementation of a linear transformation is that any desired window function (e.g., Hamming, Poisson, Gaussian, Dolph-Tchebyshev, or Kaiser-Bessel)[9] can be incorporated directly in the transparency itself with no need of any additional electronic or optical components.

Current Configuration

The most compact implementation of the electro-optical processor is with the matrix mask in direct contact with the photosensitive CCD surface.* Because of the small dimensions of the CCD photosites (typically 1 mil by 1 mil) very close contact ($\ll 1$ mil) is required in order to minimize smearing due to optical diffraction. This, and the necessity for critical alignment, strongly suggest that the mask should be fabricated directly on the CCD surface itself, as a final step in the CCD fabrication process. This yields a CCD with an integral pre-aligned matrix mask.

In 1977, RCA Laboratories (David Sarnoff Research Center, Princeton, New Jersey) under contract to the Naval Ocean Systems Center (San Diego, California) fabricated masks onto RCA's commercially available model SID 52501 CCD. These devices have K=512 by M=320 resolution cells on 1.2 mil centers. The first step in the process was the preparation of a photolithographic mask containing the desired 512 by 320 element matrix of apertures, $h_{m,k}$. The remaining steps consisted of (1) depositing a protective oxide layer on the CCD structure, (2) depositing an opaque 1200 Å thick chromium film onto this layer, (3) imaging the photolithographic mask onto this film and etching away the mask apertures using standard photoresist techniques, and (4) covering the resulting device with a protective 10,000 Å thick SiO_2 layer. The range of aperture sizes achieved in this effort was 100 discrete distinguishable levels and improvements in the technique are in progress to push this to about 256 discrete levels.

With such a "masked CCD" the only remaining component in Figure 1 is the illumination device. Successful results have been obtained with both the Monsanto MV-4 visible LED and the Texas Instruments TIXL 12 P-N Gallium Arsenide infrared-emitting diode. The electro-optical processor geometry shown in Figure 3 has proven highly attractive since (a) it maximizes the optical path from the LED to the CCD

*For those applications requiring programmability of the matrix, the mask may take the form of a photographic transparency imaged onto the CCD via imaging optics or fiber optics.

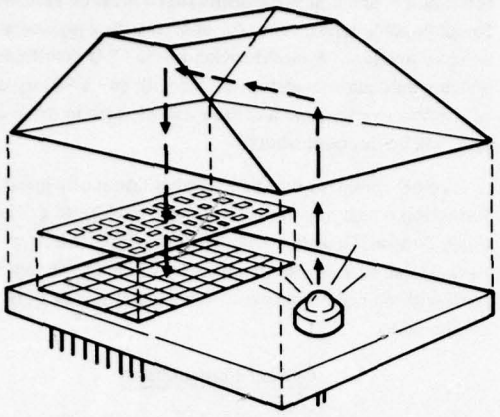

Figure 3. Current configuration for the fixed-mask electro-optical signal processor.

(thereby maximizing the uniformity of illumination) for a given module height by using a folded optical system, (b) its total volume is only two cubic inches, and (c) the CCD and LED electrical contact pins are on the same side, thereby permitting the unit to be readily soldered in place on a circuit board.

This processor is currently being tested and evaluated. Factors which adversely affect performance and which therefore need to be measured and controlled, are

- LED linearity,
- spatial uniformity of illumination,
- CCD spatial variations in sensitivity,
- CCD charge transfer efficiency, and
- CCD dynamic range.

Expected performance parameters are

$V_{in} = V_{ver}$ = 32,000 samples/sec

V_{hor} = 10,240,000 shifts/sec

dynamic range > 50 dB

nonlinearity < 1% .

Such a processing module has a processing rate of $32{,}000 \times 512 \times 320 \approx 5 \times 10^9$ multiplications/sec.

A Modified CCD Architecture

As discussed earlier, this electro-optical processor multiplies every possible time shift, n_o, of a K-point window of the input signal f_{n_o+n} by the M different K-point reference signals $h_{m,k}$ on the mask as described by Eq. (1). This "sliding window" operation is vitally important in the multi-channel cross-correlation application but is very wasteful in the FIR filtering and linear transformation applications. The overlap factor between successive windows is given by (K−1)/K which, for K=512, is 99.8%. Contrast this with the 50% overlap factor typically used in most Fourier transform operations where a good window function is used. Thus, the successive rows of data g_{m,n_o} coming out of the CCD contain highly redundant information. In other words, if we view a Fourier transformer as a bank of parallel band-pass filters we can sample the filter outputs at a sample spacing equal to the inverse of the length of the window function used; whereas the electro-optical processor samples them at the input signal sample rate. That is, the processor gives one complete row of Fourier coefficients out for each new sample value read in.

It is relatively trivial to re-sample the coefficients coming out of the CCD, i.e., to consider only every $K/2^{th}$ row if a 50% overlap factor is desired, but this still leaves the processor's input rate limited to v_{hor}/M (i.e., to 32,000 samples/sec for the components in the current implementation). The bottleneck in throughput rate is the on-chip parallel-to-serial converter. The vertical registers of the CCD are capable of shifting much faster than v_{hor}/M shifts/sec but are restricted to this rate by the time required to read each row of samples out of the horizontal shift register. A vertical shift rate faster than v_{hor}/M would result in charge packets from the succeeding row of coefficients being added to the desired coefficients shifting across the horizontal register. Such contamination would severely degrade the desired coefficients.

What is needed is a way of discarding the unwanted rows of data coming out of the tops of the vertical shift registers without contaminating the desired row being read out of the horizontal register. This could be achieved by incorporating a "controllable charge dump" gate structure between the vertical and horizontal registers. This would allow all unwanted output vectors g_{m,n_o} to be dumped to ground except when a predetermined trigger is applied to route the desired row of values into the horizontal register. To this end, the Naval Ocean Systems Center, under sponsorship from the Naval Electronics Systems Command, Code 304, is currently requesting proposals to design and fabricate such a modified CCD architecture in FY 1979.

For a square CCD array (i.e., M=K), this would allow v_{ver} (and consequently v_{in}) to be equal to v_{hor}. This case is depicted in the timing diagram of Figure 4 and corresponds to adjacent-window transformations (i.e., overlap factor = 0).

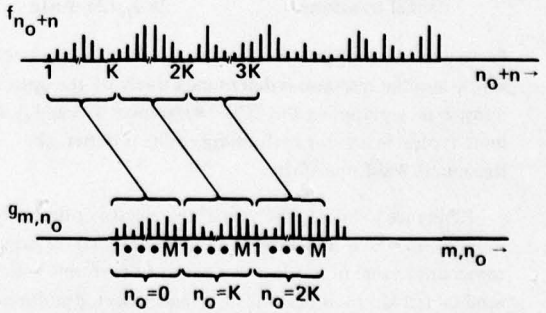

Figure 4. Timing relationship between input to LED and output from CCD for the case of adjacent-window transformations (i.e., M=K and $v_{ver} = v_{hor}$).

This would provide a compact, inexpensive Fourier transform module, for example, capable of processing input data rates as high as 10 MHz. Any arbitrary degree of window overlap can be provided for any arbitrary CCD size (i.e., any arbitrary M and K) by appropriate selection of v_{ver} and v_{hor} as shown in the generalized timing diagram of Figure 5.

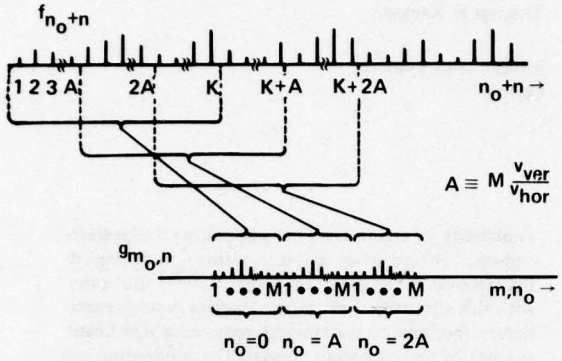

Figure 5. Timing relationship between input to LED and output from CCD for the case of transformations with arbitrary overlapping of windows. Overlap factor = $(K - M\, v_{ver}/v_{hor})/K = (v_{hor} - v_{ver})/v_{hor}$ for K = M.

Conclusions

This paper has qualitatively described a new signal processing module capable of performing a variety of useful operations at high speeds and in a compact package. However, possibly the best feature of such devices is their potential low cost. As CCD yields increase, their prices will drop, thus yielding electro-optical processors costing only a few hundred dollars.

Acknowledgements

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THE EOP – A CCD-BASED ELECTRO-OPTICAL PROCESSOR*

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Introduction

The electro-optical processor (EOP) developed by the authors is a compact, flexible device designed for use in many signal processing applications. Prior advances have been described in references 1–6. This paper will provide an overview of the history and mathematical basis of the device, present the current state of implementation, and indicate promising new investigation areas.

The EOP consists of an incoherent light source (e.g., an LED), a photo-generated mask, and an area-array charge coupled device (CCD). The package which encloses these elements is approximately two cubic inches in volume. Supporting circuitry is contained on three printed circuit cards. The current implementation is capable of performing 5×10^9 analog multiplications per second.

Development History

During the mid-1960's the scientific literature on optical signal processing emphasized the usefulness of *coherent* optical methods in performing various mathematical operations such as two-dimensional Fourier transforms and matched spatial filtering. Investigations in this regard have continued, at an increasing pace, with good results achieved. Somewhat later, investigators, disturbed by the expense, size, and critical environmental controls usually necessary in coherent systems, recognized that in some applications a non-coherent approach could be substituted. This involves simply decomposing all complex bipolar signals and operations into their real non-negative parts, as is done in digital computers, thereby eliminating the need to operate directly with complex quantities.

Early in the development of non-coherent optical processors, systems utilizing television cameras and line-array CCD's in conjunction with oscillating mirrors were successfully demonstrated.[1,2,3] The availability of area-array CCD's operating in the shift-and-add (or time-delay and integration) mode permitted removal of the oscillating mirrors.[4,5,6] But even with this elimination of the mechanical moving parts these experimental systems still required a significant amount of space to accommodate the condensing and imaging optics necessary to image the mask onto the face of the CCD. Now, the masks are fabricated directly onto the CCD obviating the need for any lenses and thereby allowing non-coherent processing modules to be packaged in just a few cubic inches.

Mathematical Basis

The generalized equation for a linear transformation

$$\int h(m,n)\, f(n)\, dn = g(m) \tag{1}$$

can be rewritten in its discrete form as

$$\sum_{n=1}^{N} h_{m,n}\, f_n = g_m \quad . \tag{2}$$

This can be further stated as a series of sums of products,

$$\sum_{n=1}^{N} h_{1,n}\, f_n = g_1 \quad ,$$

$$\sum_{n=1}^{N} h_{2,n}\, f_n = g_2 \quad ,$$

$$\vdots$$

$$\sum_{n=1}^{N} h_{M,n}\, f_n = g_M \quad . \tag{3}$$

*Published in the Proceedings of the 1978 International Conference on the Application of Charge Coupled Devices, San Diego, California, 25-27 October 1978.

Some of the forms of the matrix $h_{m,n}$ used to perform various linear transformations are

Impulse Response	Transformation
h_{m-n}	Convolution
h_{n-m}	Cross-correlation
f_{n-m}	Autocorrelation
$\cos(2\pi mn)$	Cosine transform
$\exp(-2\pi imn)$	Fourier transform
$\exp(-mn)$	Laplace transform
$2\pi J_o(2\pi mn)n$	Hankel transform

The EOP, as shown schematically in Figure 1, performs any of these transformations as determined by the mask inserted between the LED and the CCD. That is, each of the M columns of the mask and CCD performs one of the M sums of products of Eq. (3). The following paragraphs qualitatively show the EOP's operation. References 4 and 5 contain a more rigorous analysis.

In the EOP, the multiplications indicated occur as light passes through a partially transparent mask containing the matrix $h_{m,n}$ as its transmittance function. The intensity of the light emanating from the mask is indeed the product of the irradiance of the original light and the intensity transmittance of the mask. Summation occurs through the ability of the CCD to convert these photons into charge packets, with a direct linear relationship between total light impinging on a cell and the amount of charge accumulated. By shifting the charge packets vertically upward by one resolution cell per input sample to the LED, addition of the proper terms through the addition of these charge packets is accomplished.

To illustrate the principal of operation consider the most trivial cases in which M = 1 (i.e., consider only a single column of the mask and CCD) and N = 3. The light source is consecutively intensity modulated by three input samples f_1, f_2, and f_3. This light illuminates a mask with transmittance values h_1, h_2, and h_3 and falls upon the three CCD cells c_1, c_2, and c_3. Since the incoming light floods the mask, at the end of the first period the charge in cells c_1 through c_3 is proportional to f_1h_1, f_1h_2, and f_1h_3 respectively. After a shift of packets from c_1 to c_2, c_2 to c_3, and from c_3 out to the horizontal shift register, and another flood illumination by the input signal f_2, the charge in cells c_1 through c_3 is proportional to f_2h_1, $f_1h_1 + f_2h_2$, and $f_1h_2 + f_2h_3$. Another shift and illumination yields three charge packets proportional to f_3h_1, $f_2h_1 + f_3h_2$, and $f_1h_1 + f_2h_2 + f_3h_3$. Upon the next shift, this last value is shifted into the horizontal shift register and read out of the CCD. It should be recognized as one of the sums of products of Eq. (3). By extension, it can be seen that an M X N resolution-cell CCD, with an appropriate mask can be used to generate a series of M sums of N products.

To continue the trivial example considered above, if a fourth input sample modulates the LED and a fourth shifting of charge packets takes place, the resulting values in c_1 through c_3 will be proportional to f_4h_1, $f_3h_1 + f_4h_2$, and $f_2h_1 + f_3h_2 + f_4h_3$. This last value, which will be read out of the CCD on the next vertical shift, is again one of the sums of products of Eq. (3) but with the time variable of the input sequence incremented by one. After the initial

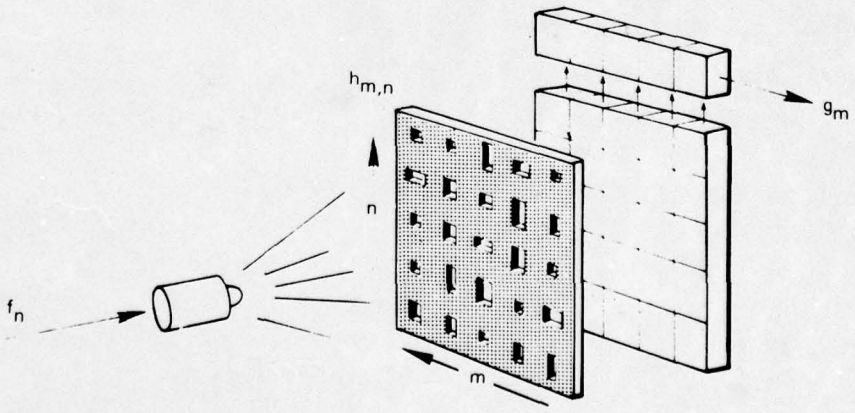

Figure 1. An Electro-Optical Processor (EOP).

start-up transient, each new input sample to the EOP produces a set of sums of products terms of Eq. (3) but where the summation takes place over the *previous* N input samples. In other words, the EOP performs *sliding-window* transformations. Or, in a pattern recognition operation, the EOP generates the complete cross-correlation *function* (i.e., the cross-correlation *value* for all time delays) between the input and each member of the library of reference signatures on the mask.

It was mentioned earlier that signal decomposition was required in those classes of linear operations which call for both real and imaginary and/or positive and negative components. In the EOP, this decomposition is achieved by using separate areas of the mask for each component, and by biasing the light source, with the results appropriately combined by electronic circuitry at the output of the CCD.[6]

Current State Of Development

In 1977, RCA Laboratories (David Sarnoff Research Center, Princeton, New Jersey) under contract to the Naval Ocean Systems Center (San Diego, California) fabricated masks onto RCA's commercially available model SID 52501 CCD. These devices have N = 512 by M = 320 resolution cells on 1.2 mil centers. The first step in the process was the preparation of a photolithographic mask containing the desired 512 by 320 element matrix of apertures $h_{m,n}$. The remaining steps consisted of (1) depositing a protective oxide layer on the CCD structure, (2) depositing an opaque 1200 Å thick chromium film onto this layer, (3) imaging the photolithographic mask onto this film and etching away the mask apertures using standard photoresist techniques, and (4) covering the resulting device with a protective 10,000 Å thick SiO_2 layer. The range of aperture sizes achieved in this effort was 100 discrete distinguisable levels and improvements in the technique are in progress to push this to about 256 discrete levels.

Figure 2 shows a corner of the resulting "masked CCD". It is interesting to note the three-phase electrode structure of the horizontal shift register at the top of the photograph and the electrode structure (3 electrodes per resolution cell) of the vertical registers showing through the transparent apertures of the mask.

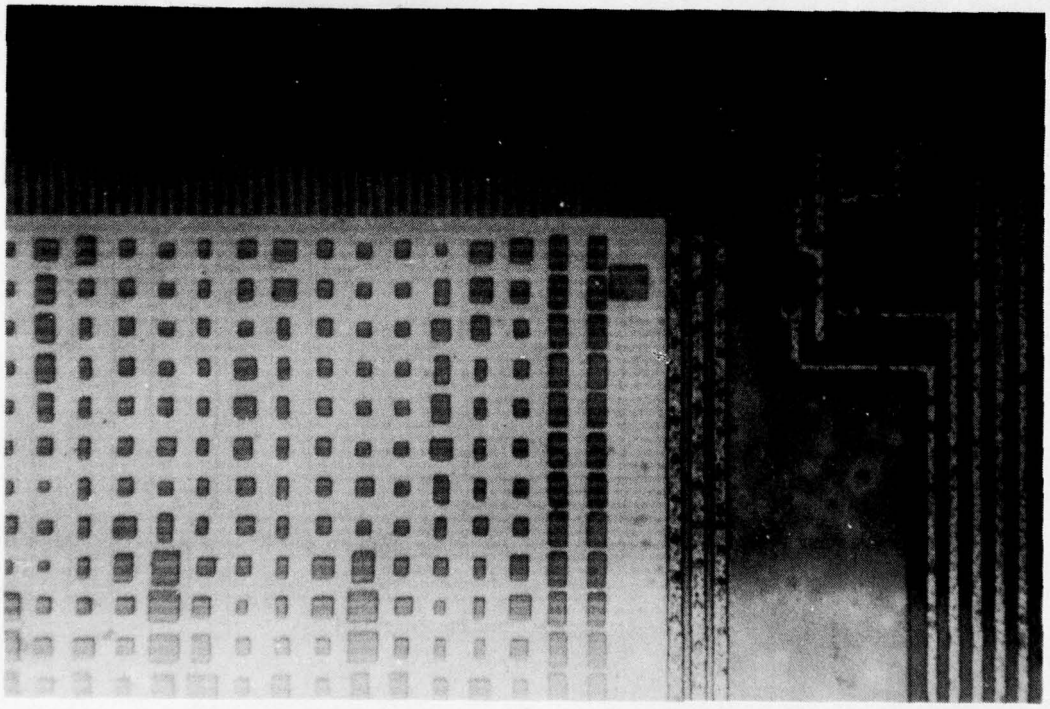

Figure 2. Photomicrograph of a corner of the mask/CCD combination.

With such a "masked CCD" the only remaining component in Figure 1 is the illumination device. Successful results have been obtained with the Monsanto MV-4 visible LED. The housing which holds the LED and CCD also serves as an optical cavity to help provide a uniform illumination across the CCD surface. Several optical cavity geometries are currently being theoretically and experimentally investigated with respect to maximizing uniformity and efficiency in a minimum size. As discussed more fully in reference 7, both the cylindrical and spherical geometries with appropriately placed baffles appear capable of reducing illumination nonuniformities across the CCD surface to under 1% in a housing size of 2 cubic inches.

This processor, with a cylindrical cavity geometry, is currently being tested and evaluated. Factors which adversely affect performance and which therefore need to be measured and controlled, are

- LED linearity,
- spatial uniformity of illumination,
- CCD spatial variations in sensitivity,
- optical crosstalk between CCD cells
- CCD charge transfer efficiency, and
- CCD dynamic range.

Expected performance parameters are

$v_{in} = v_{ver} = 32{,}000$ samples/sec
$v_{hor} = 10{,}240{,}000$ shifts/sec
dynamic range > 50 dB, and
nonlinearity $< 1\%$.

Such a processing module has a processing rate of $32{,}000 \times 512 \times 320 \approx 5 \times 10^9$ multiplications/sec.

The following section discusses the external circuitry designed to drive this EOP unit. No attempt has been made to miniaturize this circuitry; instead the intention has been to produce a general-purpose module in which changes in timing and operation could be incorporated by simple rewiring or changing a few components without the need for new printed circuit boards. This modular design approach, in which the circuitry used to operate the EOP as, say, a Fourier transformer is only a slightly modified version of that used to operate the EOP (with a different mask) as, say, a multi-channel cross-correlator, has saved considerable time in fabricating and verifying new processing systems.

An Overview of System Implementation

In the present implementation, the external circuitry required to operate the EOP is partitioned into three functional subsystems. These are: (1) master timing, (2) processor driving, and (3) signal conditioning. As their names imply, the master timing circuit provides the required synchronization signals for the overall system, the processor driver controls the LED operation and generates the necessary clocking waveforms for the CCD, and the signal conditioner refines the CCD read-out to be suitable for display and/or further processing. Each subsystem occupies one 10 in. by 4 in. printed circuit card. In the following paragraphs, the function and design of each card is described in detail.

Master Timing

There are two functions for the master timing card. First, it defines the clocking intervals for CCD operation. Therefore in this respect, the design is device dependent. The RCA CCD (SID52501) employed requires both vertical and horizontal clocks to operate. The alternating intervals of vertical and horizontal clocks comprise the Horizontal Gate as shown in Figure 3. The vertical clock is active only between the horizontal clock intervals.

Secondly, the master timing provides the markers required to relate the CCD read-out to the mask columns or references. The CCD read-out is the computational result, g_m, from the EOP; that is, it is a sequence of M-element vectors in the form of

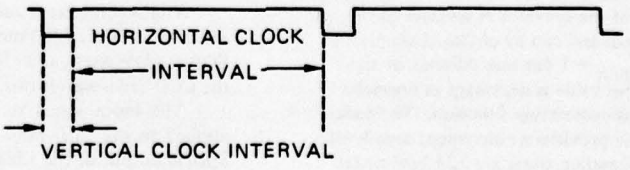

Figure 3. Horizontal Gate.

a time-varying analog waveform. These markers enable the system to recognize which point in time on this analog waveform represents the result of the running sum of products of the input sequence f_n and the m^{th} mask column. The numbers and kinds of timing markers required are application dependent. The card under discussion is designed for general-purpose usage, in that only minor wiring modifications are required to provide the markers appropriate for, for example, spectrum analysis, finite impulse response (FIR) filtering, or cross-correlation operations.

This card provides the following outputs:

(1) Horizontal Gate, shown in Fig. 3. This defines the active horizontal clock interval with a duration of 323 horizontal clock pulses and the active vertical clock interval with a duration of 7 horizontal clock pulses. (Each horizontal or vertical clock pulse results in one shift along the horizontal or vertical register respectively. However, as will be discussed later, a vertical clock pulse occupies 7 horizontal clock periods.)

(2) Valid Row Gate. This defines the location of the desired rows of the CCD output. In many applications only certain rows of outputs are wanted. For example, in an EOP performing a 512-point Fourier transform with a 75% window-overlap factor, only every 128^{th} row of output Fourier coefficients, g_m, would be desired.

(3) Valid Column Gate. This defines the location of the desired columns in the CCD read-out line. In many applications, only a specific sequence of columns are wanted. For example, in a spectrum analyzer, one may be interested in only a subset of the frequency components, or in a cross-correlator, one may wish to ignore the columns used to obtain normalization constants and zero levels.

(4) Normalization & Dark-Level Pulses. These are time signals indicating where the normalization value and dark-level value occur on a line basis. The former is simply the sum of the previous N samples of the input signal and can be obtained simply by letting $h_{m,n} = 1$ for one column of the mask. This value is necessary in normalizing a cross-correlation function. The dark-level value provides a convenient zero level. As stated earlier, there are 323 horizontal clock pulses, and 322 states in the horizontal register of the CCD. The one extra clock pulse is for shifting out the video black level (containing only thermally generated "dark current") to be used for dc restoration.

(5) Frame Synchronization Pulse. This occurs at the start of each 512-line frame and has a duration of one line (i.e., one period of the Horizontal Gate). A Frame Time is the time required to shift a charge packet from the bottom to the top row of CCD cells. When the electro-optical processor is operated in the so-called TV mode, for initial check out purposes, the Frame Synchronization Pulse is used as the input to the LED so that the LED flashes on only once during the entire frame. Conveniently, this results in an image of the mask being read out from the CCD (i.e., each mask column has been correlated with a Dirac delta function thus the correlation output is the mask pattern itself).

The circuitry to provide these outputs is shown in Figure 4. It consists of two sections: the horizontal clock section and vertical clock section – each composed of counters, decoders and combinatorial logic.

The basic horizontal timing is maintained by a set of horizontal counters. They provide 330 distinct clock periods. With this configuration, any of the 330 clock periods composing the line can be pinpointed by the use of decoders and logic circuits. In this manner, the various horizontal timing signals are generated. Furthermore, the horizontal section produces a vertical pulse occurring at the line rate. This pulse is used to increment the line counters in the vertical section to maintain 512 distinct line periods. The counter output is decoded to produce the Frame Synchronization Pulse and the Valid Row Gate. Additionally a high frequency clock running at four times the horizontal clock frequency is available for producing the three-phase horizontal clocks in the processor driver card.

Processor Driver

The second card, called the processor driver, contains: (1) the LED modulation circuitry, (2) the EOP module itself, and (3) the circuitry to generate the CCD drive waveforms.

The input signal to the processor system is applied to the LED modulator which controls the optical output of the LED. The EOP module contains the LED and the masked CCD enclosed in an optical cavity, as described in an earlier section. The waveform circuitry is divided into the horizontal and

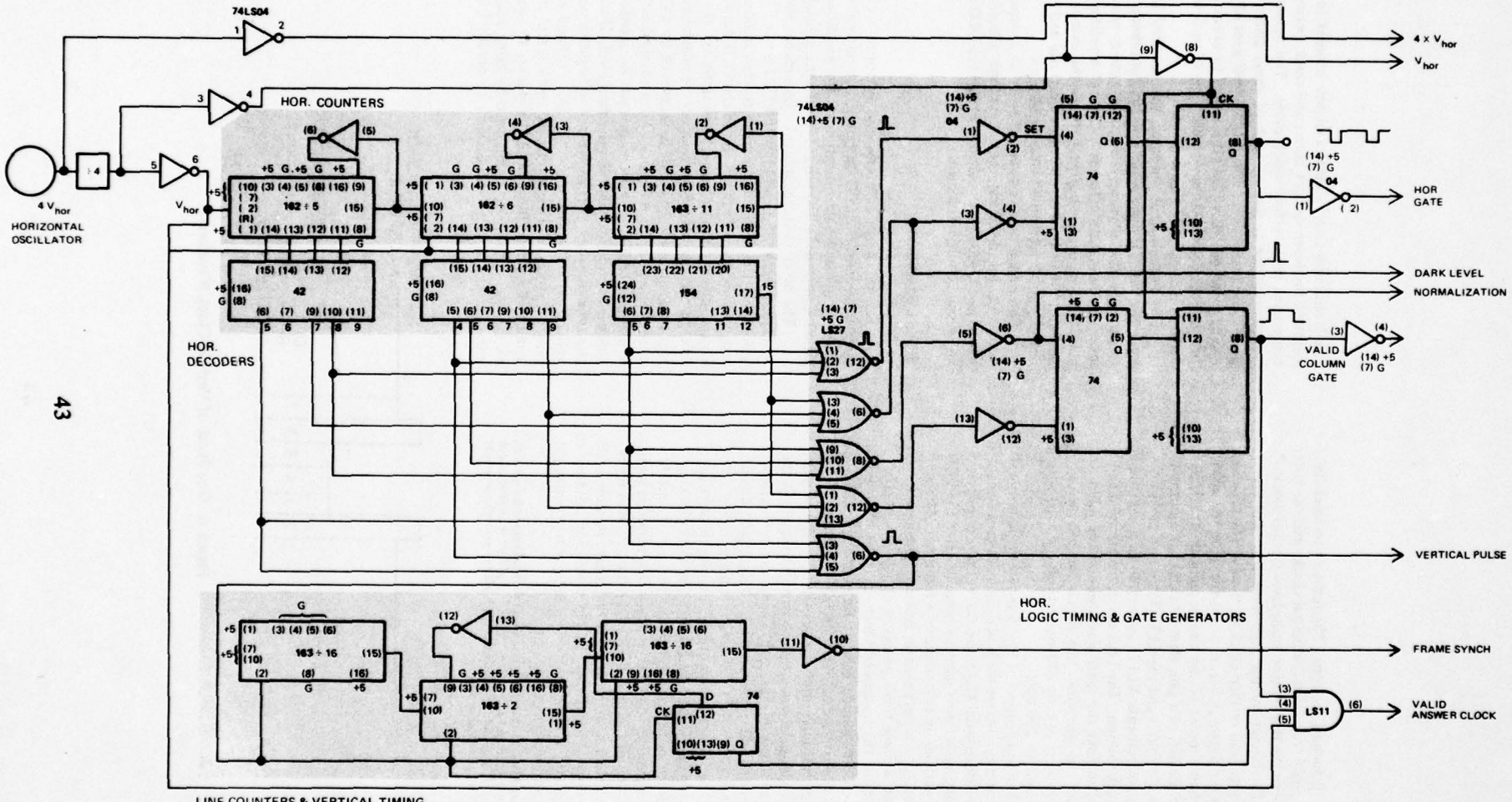

Figure 4 Master timing.

vertical clocking sections. The former produces the three-phase, two-level horizontal clocks and the latter produces the three-phase multi-level vertical clocks.*

The circuit for the LED modulator and the horizontal and vertical clock sections of the processor driver are shown in Figure 5. As shown in the upper right hand corner of the circuit diagram, the LED driver consists of a gain element (LF357), a current driver (LH0002) and the LED (Monsanto MV4 or Texas Instruments XL12) connected in a negative feedback fashion. The LED current is sampled and forced to have the same waveshape as the input voltage. In operation, this circuit can produce a current pulse of 0 to 100 ma through the LED with a rise time of 200 nsec.

The top portion of Fig. 5 shows the horizontal clock section. After the horizontal clocks are enabled by the Horizontal Gate, the three-phase two-level clocking waveforms used to actually drive the CCD are generated by two stages of a flip-flop (74LS74) connected in a shift-register fashion. The amount of overlap among these phases is controlled by the phasing of the horizontal clocks and the 4X clocks (i.e., clocks running at four times the horizontal clock rate). Clock drivers (DS0026) are used to provide the horizontal drive capability. The outputs of the clock drivers are capacitively coupled to the CCD so that a dc bias to the clocks can be inserted. The entire waveform can be shifted up and down with respect to the CCD substrate bias.

The lower portion of Fig. 5 shows the vertical clock section. Each cycle of the vertical clocking waveform occupies the time of seven horizontal clock periods. Thus the vertical clock period is seven times that of the horizontal clock (i.e., It takes seven times longer to transfer all of the charge packets in the CCD vertical registers up by one resolution cell than to transfer those in the horizontal register to the right by one cell).

*The processor driver circuitry described herein is designed for use with the aforementioned RCA SID 52501 CCD. For a more detailed discussion of the required waveforms than space permits here, please refer to the RCA specifications sheet.

The Horizontal Gate enables a binary counter to maintain the seven district horizontal clock periods comprising each vertical clock cycle. The signals representing the timing of each of these distinct periods are logically combined to control a set of four analog switches (RCA CD4016), inputs to which are fed with the desired voltage levels. One of such waveforms is illustrated in Figure 6.

For experimental purposes, the circuitry to generate the CCD drive waveform has been made very flexible thereby allowing changes in various voltage levels to be readily effected. Current amplifiers (LH0002) are used as buffers between the switch outputs and the CCD. This circuit exhibits rise and fall times from -2 volts to +7 volts of 50 nsec.

Since each card is designed to be an independent unit, for modularity considerations, a buffer amplifier (LH0033) is used to interface the CCD with the signal conditioning card.

Signal Conditioner

The signal conditioning card performs: (1) amplification of the CCD output, (2) dc restoration, (3) a sample-and-hold operation on the amplified signal; and provides (4) output interfacing capability.

The detail circuit and block diagrams are shown in Figure 7. A vido amplifier (μA733) is used for amplifying the CCD output from the ten millivolt range to the one volt range. Since the CCD output is capacitively coupled through the amplifier, the dc level of this resulting signal needs to be re-established. It is convenient to utilize the dark level of the CCD output as a point of reference. As mentioned earlier in the master timing section, an extra horizontal clock is provided to shift out the dark level. During this time, the dark level is clamped to negative one volt by use of an analog switch (DG 187) and amplifier (LH0033). The dc restored signal is still contaminated by feed-through of the clocks, so these extraneous signals must be removed by using a sample-and-hold amplifier (Datel SHM-2) to obtain the

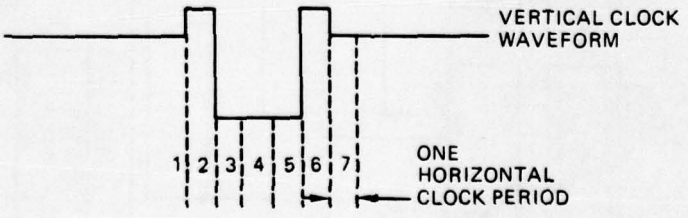

Figure 6. One Phase of Vertical Clock Waveform.

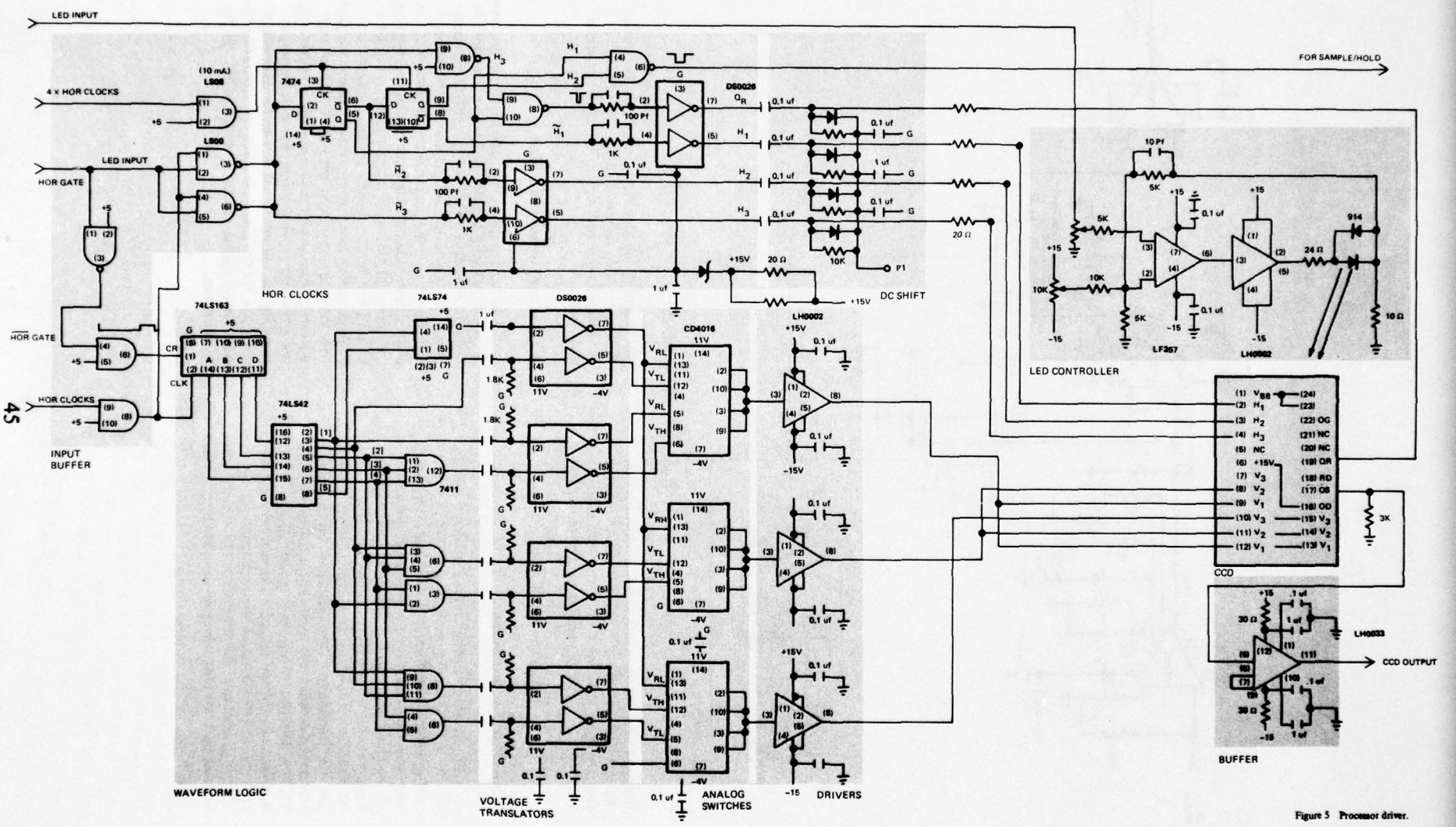

Figure 5 Processor driver.

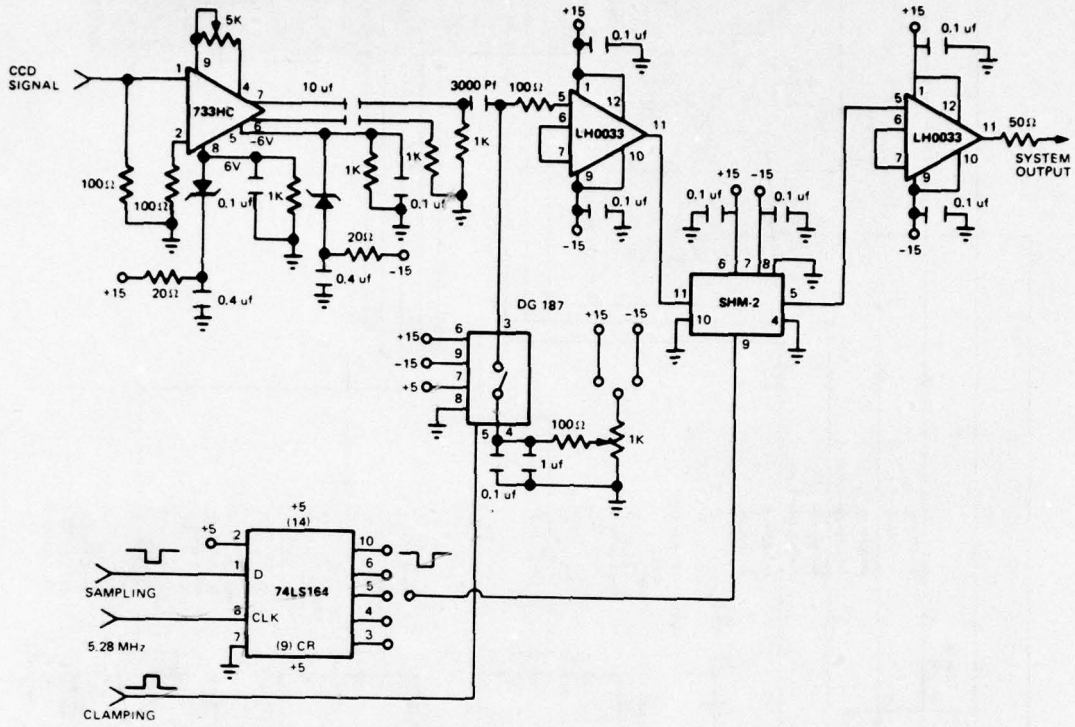

Figure 7. Signal Conditioner.

desired analog signal – 320 sampled values per row. Again a buffer amplifier (LH0033) is used to interface the sample-and-hold unit with any external load for output display and/or further processing.

New Investigative Areas

A Modified CCD Architecture

During the discussion of the mathematical basis for the EOP, it was shown that the EOP performs *sliding-window* transformations. In those cases where large window overlap is desirable, for instance when an incoming signal has some arbitrary unknown starting point, this feature is very useful. In those cases where little window overlap is desired some mechanism for flushing out the unwanted coefficients (thereby increasing the bandwidth capability of the EOP) is desired. To this end, industry has been approached for solutions, such as a selectable gating function inserted between the area array and the output parallel to serial converter.[8] If successful, the vertical shift rate (and therefore the input sample rate) will become much less dependent on the horizontal shift rate, and in fact, limited only by CCD shift drive capabilities and electro-optical input signal generation.

A Real-Time Programmable Mask

Another promising investigative area is the mask. It is obvious that if a method of generating masks in real time or near real time existed, additional operations could be performed, such as non-linear transformations, recursive algorithms, adaptive solutions, and multi-stimulus correlations. Technologies being considered at this time include matrix-addressed transmissive liquid crystal devices. Laboratory demonstrations have been performed using a Hughes liquid crystal cell imaged onto the CCD, but considerable advancement must be made in expanding the grey scale capability (i.e., dynamic range), in reducing the resolution cell size to be compatible with that of CCD's, and ultimately in fabricating the transmissive matrix-addressed mask directly on the CCD surface.

Digital Capability

The last area to be discussed is that of digital operations with this unit. Historically, optical processing has been considered only applicable to analog problems with accuracies corresponding to about 8 bits, but work is proceeding with mask design and supporting algorithms to permit digital operations with any desired degree of accuracy.

Conclusion

The EOP is a compact, low-cost, low-power, high-speed signal processing module capable of performing a larger variety of useful linear operations with processing rates greater than 10^9 multiplications per second (depending on the array size and maximum vertical shift rate of the CCD used). General-purpose modules, each consisting of a two cubic inch EOP and three cards of external circuitry, have been fabricated and are now undergoing test and evaluation in a variety of application areas. Also, further development work is planned to increase the EOP's input rate from the present 32 kHz to the MHz range, to provide real-time programmability of the mask, and to allow the performance of digital operations with arbitrary accuracy.

Acknowledgements

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APPENDIX B

Data Sheet on Reticon's CCD Transversal Filter

KEY FEATURES

Provides the real and imaginary convolutions necessary for the chirp Z transform algorithm.

Two 512-stage charge-coupled devices.

Four mask-programmed transversal filters.

Balanced differential outputs.

Dynamic range (peak signal to rms noise) of 60 db.

Sampling rates 4 KHz to 2 MHz.

Filter weighting coefficient accuracy of eight bits plus sign.

22-pin dual-in-line package.

INTRODUCTION

The R5601 is an MOS integrated circuit which can be used to perform the bulk of the computation required in the calculation of a 512-point Discrete Fourier Transform (DFT).[1] This circuit contains two separate 512-stage charge-coupled devices which are used to implement four transversal filters using the split-electrode weighting technique.[2] The filter weighting coefficients and internal circuit connections are configured so that this device, with additional off-chip components, can implement the chirp Z transform (CZT) algorithm to calculate a 512 point DFT.[2]

There are two versions of the R5601 which are available. They differ in the type of window which is effectively applied to the data to be transformed. The R5601-1 uses a rectangular window for maximum resolution in the transform (or frequency) domain with the disadvantage of relatively high sidelobe response (frequency leaks).[3] The R5601-2 uses a Hanning window in order to decrease these sidelobes. However, this window also decreases the frequency resolution of the resulting DFT by about a factor of two. In general, the R5601-2 is intended for use in spectral analysis applications and the R5601-1 for direct calculation of the complex Fourier coefficients.

The use of analog discrete time techniques to calculate Fourier spectra allows an enormous reduction in hardware complexity and, therefore, cost when compared to all-digital techniques. This approach should find application whenever low cost, reduced size, high speed, or low power requirements are important.

DEVICE DESCRIPTION

The R5601 is available in a 22-pin DIP package with connections as shown in Figure 1. The functions of the pins are given in Table I and a simplified block diagram in Figure 2. The timing diagram is shown in Figure 3 and a typical connection arrangement in Figure 4. Figures 5 and 6 depict the device geometry and the I/O circuits. The chip contains two CCD channels lying adjacent to each other. Figure 5 is an edge view of the chip which has been cut along the length of the channels to exhibit the four-phase clock gates which are driven by an external clock to transfer the signal charge. The input signal gates, I_{SGR} and I_{SGI}, for real and imaginary channels, respectively, are clocked with the same phase as ϕ_2; therefore, the signal is sampled into both channels when ϕ_2 goes low. These discrete signal packets then pass under the input receiving gates, I_{RGR} and I_{RGI}, which are the receiving gates for the real and imaginary channels respectively, then sequentially transfer down the channel through the potential wells which are formed under each of the four clock phases, ϕ_1, ϕ_2, ϕ_3 and ϕ_4, through clocks applied from an external source. After transferring through the channel, the signal terminates into V_{dd} through the output gate, V_{OG} and the switch labeled RESET. The delay line outputs, labeled VOI and VOR, are required only during testing and initial adjustment.

Figure 6 depicts the top view of a single CCD channel and demonstrates the split-electrode technique which implements the two different filters on each channel. The weighting coefficients of these filters are determined by each major gate electrode which is split with weighting proportional to the difference in the lengths. The chirp waveform in dotted lines emphasizes the two separate weighting functions on the same channel, one weighting effective during ϕ_1's high state, and the other effective during ϕ_3's high state.

In order to perform the Fourier transform, it is necessary to multiply the input signal by a complex chirp waveform, convolve the real and imaginary parts with a second complex chirp waveform and then post multiply the output by the same chirp waveform used in the pre-multiplication. The R5601 performs the convolution of the real and imaginary input signals with a complex chirp $e^{(i\pi n^2)/N}$, $1 \leq n \leq 512$ for the R5601-1. If only the magnitude of the spectrum is required, then the filter outputs are squared and summed. This is true for both the R5601-1 and R5601-2. Block diagrams for calculating the power spectra $|F_k|^2$ and the complex Fourier coefficients F_k are shown in Figure 7. The major computational task -- the complex convolution -- is performed by the R5601 convolution filter shown within the dash-line rectangle.

To perform the convolution, the R5601 device contains four 512-stage CCD mask-programmed transversal filters which are implemented using two CCD delay lines. The two different filter functions on each CCD are programmed by splitting the ϕ_1 and ϕ_3 clock electrodes which are labeled (ϕ_1^+, ϕ_1^- and ϕ_3^+, ϕ_3^-) as shown in Figure 6. The effective multiplying factor, called the weighting coefficient, is proportional to the difference in size of the two portions of a particular electrode. These weighting coefficients are programmed to an accuracy of eight bits plus sign (i.e., 512 possible levels). Since the value of the weights are determined by the pattern of one mask used in the semi-conductor fabrication process, it is expected that this accuracy level will be independent of minor fabrication variations and will be easily reproducible.

The sampled analog signal moves down the analog delay line under control of the four clock phases, ϕ_1, ϕ_2, ϕ_3 and ϕ_4 (See Figure 6). The ϕ_1 clock drive should be capacitively coupled by two capacitors to the programmed split electrodes ϕ_1^+ (Pin 6), and ϕ_1^- (Pin 4) which are also the output signal lines. This is also true for the ϕ_3 clock and the split electrodes ϕ_3^+ and ϕ_3^-. The values of the external capacitors are 500 pf. Pins 8, 11, and 15 also require the ϕ_3 clock waveform, but it should come from a different driver device than the one used for ϕ_3^+ to insure isolation of the output from the input.

The outputs from the split electrodes (i.e., ϕ_1^+ and ϕ_1^-, ϕ_3^+ and ϕ_3^-) are appropriately summed together on the chip. The output from similar clock electrodes, for example ϕ_1^+, of the two different delay lines are brought to the same point on the chip (See Figure 6). This connection performs the summing of the signals. In the typical configuration, the output from ϕ_1^+ and ϕ_1^- are differentially combined and then sampled and held until ϕ_3 data is valid. The ϕ_3^+ and ϕ_3^- are also differentially combined to produce the other output signal. Two more clock signals, ϕ_2 and ϕ_4, are minor phases required to drive these devices (See Figure 6). Two off-chip differential amplifiers with a gain of approximately 10 for the 5601-1 or 20 for the 5601-2 are required to obtain the output signals of five volts maximum amplitude.

The analog input signals into the CCD device are superposed on an approximately 6-volt dc bias level and can swing approximately four volts peak-to-peak. The input circuitry is designed to be compatible with the split-electrode output techniques to give maximum linearity and dynamic range for this device. In particular, the input structure is designed to compensate for the non-linear effects of the depletion capacitance under the CCD gates of the filter.

Pins 10 and 13 are test points. Each should be connected to a 10Kohm resistor which is connected to the substrate voltage. These pins provide the delayed value of the input signal during testing procedures.

THE TRANSFORM ALGORITHM

The complete Discrete Fourier Transform (DFT) is given by the formula

$$F_k = \sum_{n=0}^{N-1} f_n e^{-i2\pi nk/N} \qquad k = 0, 1, 2 \ldots N-1 \qquad (1)$$

where either or both F_k and f_n may be complex. The factor 2nk in the exponent can be replaced by its seemingly more complicated equivalent:

$$2nk = n^2 + k^2 - (k-n)^2 \qquad (2)$$

This substitution changes Eq. 1 to Eq. 3 below, where the pertinent factors have been segregated to emphasize the important operations.

$$F_k = e^{-i\pi k^2/N} \sum_{n=0}^{N-1} \underbrace{(f_n e^{-i\pi n^2/N})}_{g_n} e^{i\pi (k-n)^2/N} \qquad (3)$$

There are three operations indicated by Eq. 3

1. Multiply each corresponding term of the input discrete-time series, f_n, by the complex factor, exponential $(-i\pi n^2/N)$; that is, by the pair of factors $\cos \pi n^2/N$ and $i \sin \pi n^2/N$, to produce the combination term in parentheses. Let this new complex sequence be called g_n.

2. Perform a discrete convolution between the sequence g_n and the sequence $e^{i\pi n^2/N}$; this is the portion within the summation.

3. Multiply the resulting output sequence by the final factor $e^{-i\pi k^2/N}$ for each point of F_k.

These three operations are indicated in the block diagram of Figure 7, which shows the convolution portion within the dash-line rectangle. For spectral density, outputs from the convolution filter are squared and summed; for obtaining the complete Fourier coefficients, the post multiplier shown at the right in Figure 7 must be provided in place of the squaring function. For a 512-point transform, the convolution portion requires a minimum of 2048 multiplications and 2048 additions for each F_k; it thus represents the bulk of the computational task. It is this portion which is performed by the R5601 convolution filter.

Note that complex multiplication and complex convolution are linear operations; that is, operation on a sum is the same as the sum of the results of separate operations on the members of the sum. Thus, these operations can be broken into corresponding real and imaginary (quadrature) components. Note further that these operations can be handled by real operations, but in separate real and quadrature (imaginary) channels. Thus

$$x \cdot y = (x_R + ix_I) \cdot (y_R + iy_I) = (x_R y_R - x_I y_I) + i\,(x_R y_I + x_I y_R)$$

$$x * y = (x_R * y_R - x_I * y_I) + i\,(x_R * y_I + x_I * y_R) \quad \text{and} \qquad (3a)$$

$$(x \cdot y) * z = \left[(x_R y_R - x_I y_I) * z_R - (x_R y_I + x_I y_R) * z_I\right] + i\left[(x_R y_R - x_I y_I) * z_I + (x_R y_I + x_I y_R) * z_R\right] \qquad (3b)$$

These are the operations indicated in Figure 7 and Eq. 3 where $\underline{x}$ is the signal, $\underline{y}$ is the chirp multiplier and $\underline{z}$ is the convolution portion supplied by the R5601.

A general, complex input, which has separate real and imaginary (quadrature) inputs, uses the four premultipliers shown at the left in Figure 6, and a single (complex) Fourier

coefficient is obtained for each frequency component of the input. The usable input frequency band is from zero to the sample frequency, without ambiguity, because each input sample has two components (that is, there are effectively 2 f_{sample} values per second, and the Nyquist criterion thus allows a band to f_s without aliasing). Another way of viewing these results is to observe that the input premultiplier, with real and quadrature inputs, forms a single-sideband chirp modulator, so that only a single frequency occurs in the chirp input to the filter for each component of the signal.

In most cases, however, inputs are real, the imaginary input is identically zero, and two of the multipliers may be deleted. This (real) signal is simply split into two paths. The signal in one path is multiplied by a cosine chirp ($\cos \pi n^2/N$) and fed to the real channel of the filter input; the signal in the second path is multiplied by a negative sine chirp ($-\sin \pi n^2/N$) and fed to the imaginary (quadrature) channel. Each real input component, however, is composed of two complex components, one with positive frequency and one negative frequency. For example, a real signal, $f_n = \cos 2\pi nT$, is composed of complex components, $1/2\, e^{-i2\pi nT}$ and $1/2\, e^{+i2\pi nT}$, whose imaginary portions cancel. These two components generate sum and difference chirp frequencies, and for every real signal in the band 0 to $f_{sample}/2$ the negative-frequency component turns up in the band f_{sample} to $f_{sample}/2$ as an alias, thus restricting the useful input band to components lying below this Nyquist limit of $f_{sample}/2$.

The operations above will perform the complete DFT, but to do so requires careful attention to the total operation. In many cases, however, only the magnitude of the power spectrum is required (no phase information), and considerable simplification is possible. First, only the squared magnitude of the various F_k is required, so

$$\left| F_k \right|^2 = \left| \sum_{n=0}^{N-1} \left(f_n \, e^{-i\pi n^2/N} \right) e^{i\pi (k-n)^2/N} \right|^2 \tag{4}$$

The final phase multiplier term, $e^{-i\pi k^2/N}$, may be deleted because it has unit magnitude and so does not affect the amplitude. Second, it is possible to operate in a continuous fashion with only slight approximation, because so many points are involved. We step the input data each time a new spectral component is calculated. For a periodic waveform, the principal effect is a slight phase factor which has only slight effect on the result. Equation (4) then becomes:

$$\left| F_k^s \right|^2 = \left| \sum_{n=0}^{N-1} \left(f_{n+k} \, e^{-i\pi n^2/N} \right) e^{i\pi (k-n)^2/N} \right|^2 \tag{5}$$

where the designation F_k^s indicates a sliding (or continuous) chirp-Z transform[2]. The chirp-Z designation arises because of the frequency factors $e^{i\pi n^2/N}$ which effectively change frequency linearly through the interval $0 \leqq n < N$. The phase and frequency are, respectively:

$$\theta = \pi n^2/N \text{ radians}$$
$$\omega_n = \left| d\theta/dn \right| = 2\pi n/N \text{ radians/step}$$

For real inputs then, only one (common) input is used. Further, each filter pair gives one component of a complex number, so for the spectrum analyzer implementation, each component is squared, then added to the other to give the overall squared magnitude. The interior complex operations of the convolution are separated into their real and imaginary components and handled separately in the real and imaginary filter channels. This is the situation addressed by the RC5601 evaluation module which is available from Reticon. The common input f(n) is simply split into two paths for processing. The signal in one path is multiplied by a cosine chirp and delivered to one pair of convolver-filters to constitute the "real" channel; the signal in the other path is multiplied by a sine chirp and delivered to the second pair of convolver-filters to constitute the "imaginary" channel. The outputs are combined on an approximate rms basis to give the spectral density.

To see how the convolver-filters work, consider the chirped waveform of Figure 8 where the cosine chirp is plotted around the circumference of a circle to emphasize the repetitive nature of the chirp.

Only the cosine chirp is shown in the plot for clarity. Its equation is

$$r_{cos} = 2.5 + 0.5 \cos \pi\, n^2/36$$

where n = 0, 1, 2....36 and where r = 2.5 is the "axis" of the waveform. (For the figure, N = 36, to keep the figure simple; in the R5601, N = 512). Note that the waveform is accurate for $0 \leq n < N/2$, and thereafter aliasing makes the discrete points also lie on a mirror image of the first 18 points, as shown dotted, whereas the continuous chirp curve has constantly increasing frequency with many more alternations, as shown by the solid waveform.

Now consider a dc input. Multiplication by the input chirp weighting produces time samples exactly like those of Figure 8. These samples are fed into the delay line of the convolver-filters. At the end of 512 clock periods, the samples in the filter exactly match the filter, and the output is maximum at this instant in time (the zero-frequency position).

Next, consider a fixed low-frequency cosine input whose samples are $f(t) = \cos \pi\, mn/N$, with m an arbitrary (small) factor. This input is multiplied, point by point, with the cosine and sine chirps to give corresponding outputs to the filter channels of

$$P = \cos(\pi\, mn/N)\cos(\pi\, n^2/N)$$

$$= 1/2 \quad \cos \frac{\pi}{N}(n^2 + mn) + \cos \frac{\pi}{N}(n^2 - mn)$$

$$Q = \cos(\pi\, mn/N)\sin(\pi\, n^2/N)$$

$$= 1/2 \quad \sin \frac{\pi}{N}(n^2 + mn) + \sin \frac{\pi}{N}(n^2 - mn)$$

selves are chirped sum and difference frequencies just like those in
d forward or backward by the shift in frequency. Thus, we see

that there will be a new time slot, relatively earlier or later than that for dc, where the samples exactly match the filter to give maximum output. At any other position more than a small fraction of a time slot away, the match grows rapidly worse to give essentially zero output when all the weighted samples are added. Note that there is a pair of responses from the filter, corresponding to the sum and difference frequencies, since forward rotation corresponds to the sum, and rearward rotation corresponds to the difference, and matches occur due to the symmetry of the (sampled) pattern. As the input frequency is increased, the two responses move toward each other until they meet for an input at the Nyquist frequency of $f_{sample}/2$. There are thus 256 time slots where discrete frequency components can have convolution maxima, with frequency components distributed between dc and the Nyquist frequency. The resolution thus is dependent on the number of points in the matched filters. So if we have 512 points and 100 KHz sample frequency, we would end up with approximately 200Hz resolution; with 10 KHz we would have 20 cycles per sample time resolution. However, it should be noted that a frequency midway between adjacent resolution cells spreads its energy equally between the cells; in either event the area under the response tends to remain constant. Windowing, and inputs nonsynchronous with the sample rate also tend to spread the spectrum and cause it to vary in amplitude with time.

Why are there four matched filters? Equation (3b) indicates why. Even if the input is purely real (i.e., $x_I = 0$), the correlation process still requires all four components of z: two in the real channel and two in the imaginary channel. Qualitatively, for example, while a real, even input correlates primarily with the cosine chirp, the sidelobes do not cancel out nearly as well without the other filters present. For more general signals, each filter section contributes to the main correlation as well.

SPECIFICATIONS AND PERFORMANCE

The diagram of Figure 4 indicates, in part, the configuration and drive requirements of the R5601. Typical operating conditions are indicated in Table II. Input impedances to the various gates are principally capacitive in nature. The delay-line outputs are connections to active FET sources of the output source followers, so these outputs normally are connected through load resistances ($\sim$10K ohm) to the substrate potential. These delay-line outputs are normally used only during testing and initial adjustment. The delayed signal appears superposed on clock pedestals as in Figure 9 , where the cross-hatched portion represents variable values, depending on the particular signal sample. If the viewing oscilloscope sweep is synchronized to an input sinusoidal signal, the output should show a stair-step approximation to the input when biases, etc., are correctly adjusted.

EVALUATION MODULE

A printed-circuit evaluation module is available from Reticon. This module provides the external functions of clock drive, premultipliers, output buffers, squaring circuits, etc., to implement a spectral-density evaluator for real inputs. It is self-contained except for power supplies. Its design is a compromise between performance and cost, making it

useful principally for initial evaluation and simple spectral analysis. Its nominal sample rate is 100 KHz but an external input permits sampling at lower rates if desired. Further details may be found in specification data for the RC-5601 Evaluation Board.

References

(1) "The Chirp Z-Transform Algorithm", L. R. Rabiner, R. W. Schafer, and C. M. Rader; IEEE Transactions Audio Electroacoust., Vol. AU-17, pp. 86-92, June 1969.

(2) "A 500-Stage CCD Transversal Filter for Spectral Analysis", R. W. Broderson, C. R. Hewes, and D. D. Buss; IEEE Journal of Solid-State Circuits, SC-11 No. 1 (February 1976) pp. 75-84.

(3) "The Fast Fourier Transform's Errors Are Predictable, Therefore Manageable", R. W. Ramirez; Electronics, Vol 47, No. 12, June 13, 1974, pp. 96-102

Table I
R5601 Pin Functions

Pin No.	Designation	Function
1	V_{sub}	Substrate
2	ϕ_4	Minor clock for CCD transport
3	COM	Common (ground) connection
4	ϕ_1^-	(-) weights of ϕ_1 split-electrode gates
5	ϕ_{r1}	Reset gate for ϕ_1 split electrodes
6	ϕ_1^+	(+) weights of ϕ_1 split-electrode gates
7	I_{SGI}	Input sampling gate, imaginary channel
8	I_{RGI}	Input receiving gate, imaginary channel
9	Input Imaginary	Signal input, imaginary channel
10	VOI	Delay-line output, imaginary channel
11	Reset	Delay-line output reset control
12	V_{OG}	Delay-line-output-control-gate bias
13	VOR	Delay-line output, real channel
14	Input Real	Signal input, real channel
15	I_{RGR}	Input receiving gate, real channel
16	I_{SGR}	Input sampling gate, real channel
17	ϕ_3^+	(+) weights of ϕ_3 split-electrode gates
18	ϕ_{r3}	Reset gate for ϕ_3 split electrodes
19	ϕ_3^-	(-) weights of ϕ_3 split-electrode gates
20	V_{dd}	Drain supply for source-follower buffers
21	ϕ_2	Minor clock for CCD transport
22	V_{CB}	Delay-line corner-control-gate bias

Table II
Definitions and Electrical Specification

Pin No.	Functions	Parameters Symbol	Min	Typ.	Max.	Units	Note
1	Substrate	Sub	0	-1.2	-7	volts dc	3,5
2	Minor phase clock	ϕ_4	5	6	7	p-p volts	1,4
3	Common	Com	--	--	--	--	2
4	Major phase clock & Signal Output Line for Minus Signal	ϕ_1^-	10	12	14	p-p volts	1,4
5	Reset gate for ϕ_1 clock line	ϕ_{r1}	5	15	22	p-p volts	1,4
6	Major phase clock and Signal Output Line for Positive Signal	ϕ_1^+	10	12	14	p-p volts	1,4
7	Input sampling gate, Imaginary	I_{SGI}	10	15	22	p-p volts	1,4
8	Input receiving gate, Imaginary	I_{RGI}	$0.5I_{SGI}$	$0.75I_{SGI}$	I_{SGI}	volts d.c.	5
9	Signal input, Imaginary	IN-Im	2	4	7	volts d.c. (bias)	
10	Delayed output, Imaginary	VOI		see text			
11	Reset input to Channel Output Amplifier	RESET	10	15	22	p-p volts	1
12	Signal Channel Output Gate	V_{OG}	2	3	5	volts d.c.	5
13	Delayed Output, Real	VOR		see text			
14	Signal Input, Real	IN-Re	2	4	7	volts d.c. (bias)	
15	Receiving Gate, Real	I_{RGR}	$0.5I_{SGR}$	$0.75I_{SGR}$	I_{SGR}	volts d.c.	5
16	Input Sampling Gate, Real	I_{SGR}	10	15	22	p-p volts	1
17	Major Phase Clock & Signal Output Line for Positive Signal	ϕ_3^+	10	12	14	p-p volts	1,4
18	Reset clock for ϕ_3 clock line	ϕ_{r3}	5	15	22	p-p volts	1,4

Table II (continued)
Definitions and Electrical Specification

Pin No.	Functions	Symbol	Parameters Min	Typ	Max	Units	Note
19	Major Phase Clock & Signal Output Line for Minus Signal	ϕ_3 -	10	12	14	p-p volts	1,4
20	Supply voltage for output	V_{DD}	8	15	22	volt d.c.	1,5
21	Minor phase clock	ϕ_2	5	6	7	p-p volts	1
22	Corner bias	V_{CB}	2	3	5	volts d.c.	1,5

Note:
1. All clocks swing from *0 to 0.4 volts low to a high* as specified.
2. Common is reference level for all voltage measurements and is normally grounded.
3. The substrate must be at lowest potential, normally -1.2 volts.
4. See figure for clock waveform and timing; note that all waveforms must be free from over and under shoots with edges as clean as possible.
5. These are bias input nodes and must be well by-passed.

Table II (cont.)
Specifications (25°C)

INPUTS

Signal Inputs	Symbol	Typical	Units
Bias Level	Input Real	6	volts
Signal Level	Input Imaginary	4	volts (p-p)
Input Capacitance		5	pf
Clock & Drive			
Split-Electrode Clock Amplitude (Applied to Capacitors, see Fig. 2	ϕ_1, ϕ_3	30	volts
Electrode Clock Amplitude	ϕ_2, ϕ_4	3-5	volts
Reset Clock Amplitude	ϕ_{R1}, ϕ_{R3} Reset	12-15	volts
Clock Line Capacitance	ϕ_2, ϕ_4	200	pf
Clock/Sense Line Capacitance	$\phi_1^{\pm}$, $\phi_3^{\pm}$	500	pf
Minimum Sample Rate		4	KHz
Maximum Sample Rate		2	MHz
Drain Supply	V_{dd}	15	volts
Output Gate	V_{OG}	3	volts
Corner Gate	V_{CG}	3	volts
Substrate Bias	V_{sub}	-1.2	volts
Power Dissipation	--	.5	watts

OUTPUTS (ϕ_1^+, ϕ_1^-, ϕ_3^-, ϕ_3^+)

Signal Level (Superimposed on Clock Level)		.5	volts (p-p)

PERFORMANCE

Dynamic Range (Peak signal to RMS noise)		60	db
Linearity (Total harmonic distortion		1	%
Tap weight Accuracy		8 bits plus sign	

The weighting coefficients for the two devices are:

R5601-1 COS, SIN $\left\{ \frac{\pi (n-1)^2}{512} \right\}$ Tap Number = n, $1 \leq n \leq 512$

R5601-2 COS, SIN $\left\{ \frac{\pi (n-257)^2}{512} \right\}$ $\left\{ 1/2 \left[1 - \cos \left(\frac{2\pi (n-1)}{511} \right) \right] \right\}$ $1 \leq n \leq 512$

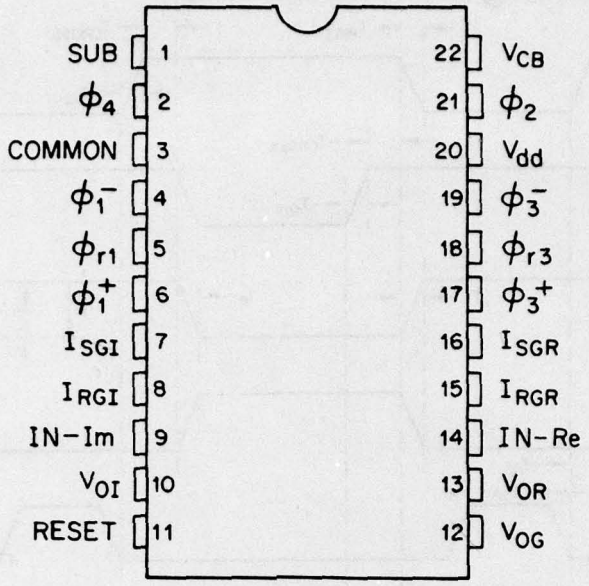


Figure 1 - Pin Designations for R5601

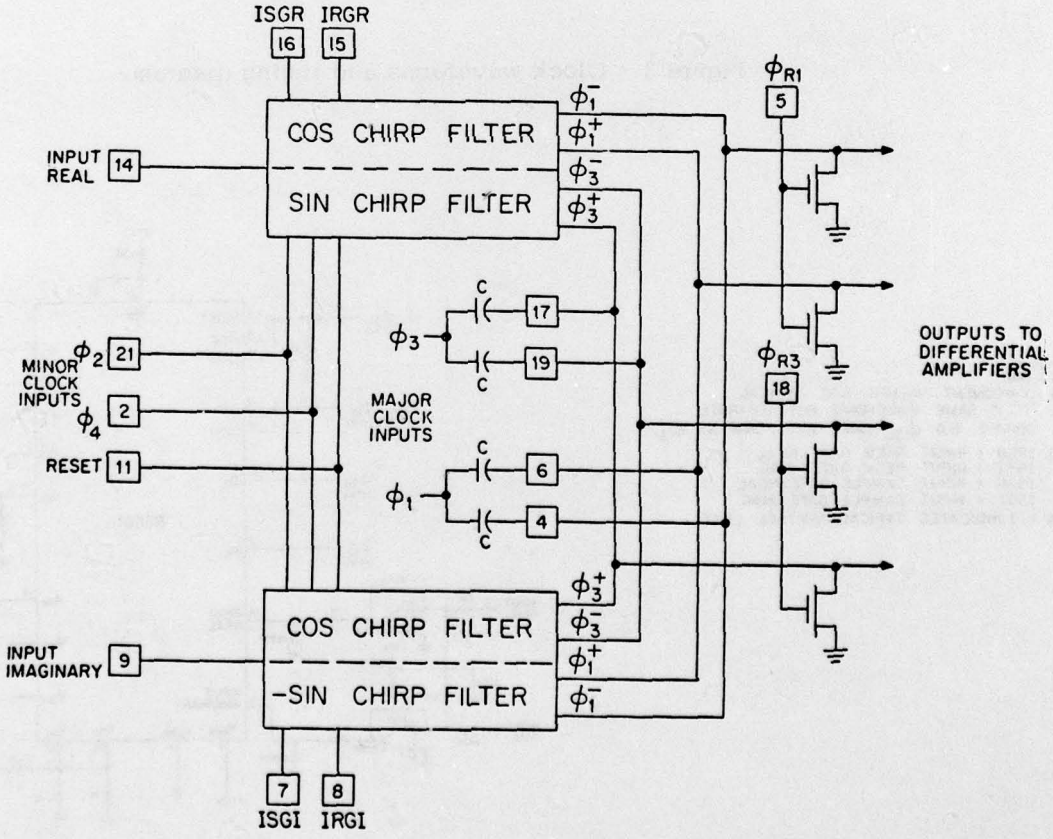


Figure 2 - Simplified Block Diagram of R5601.

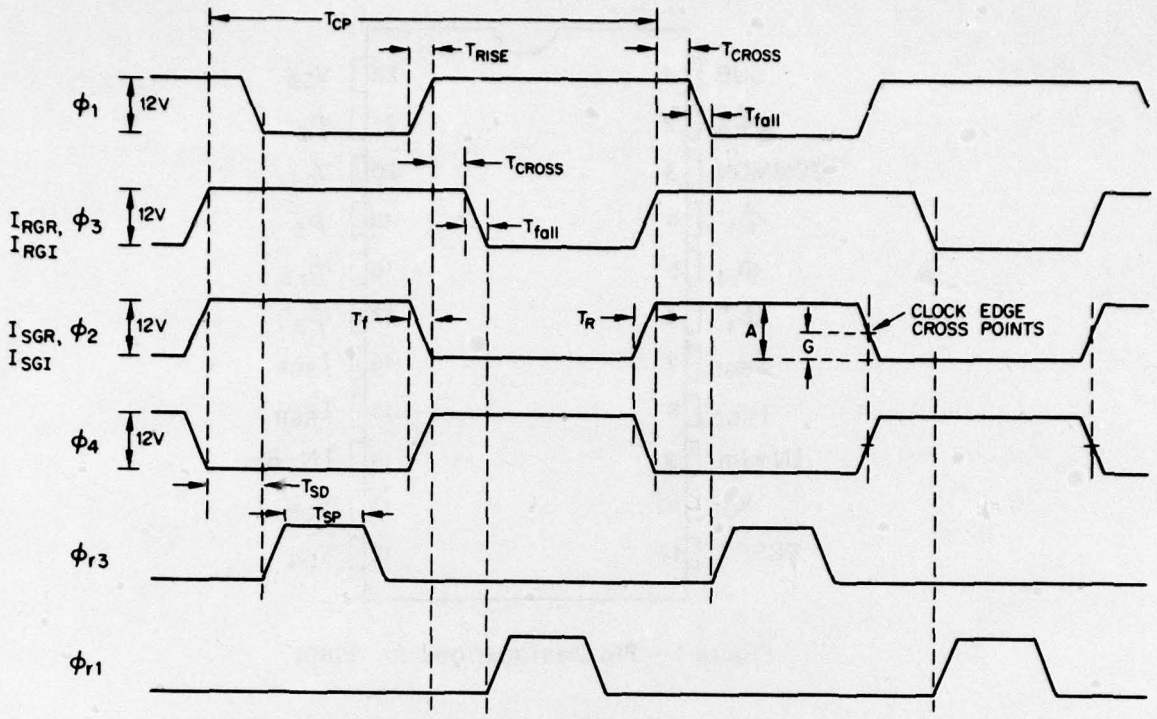


Figure 3 - Clock waveforms and timing diagram.

NOTES:

1. COMPONENT VALUES ARE TYPICAL.
2. "C" IS SAME WAVEFORM BUT SEPARATE DRIVER. E.G. ϕ_{3C} SAME WAVEFORM AS ϕ_3.
3. IRGR = INPUT RECV. GATE/REAL
   IRGI = INPUT RECV GATE/IMAG.
   ISGR = INPUT SAMPLE GATE/REAL
   ISGI = INPUT SAMPLE GATE/IMAG.
4. ( ) INDICATES TYPICAL VOLTAGE LEVEL

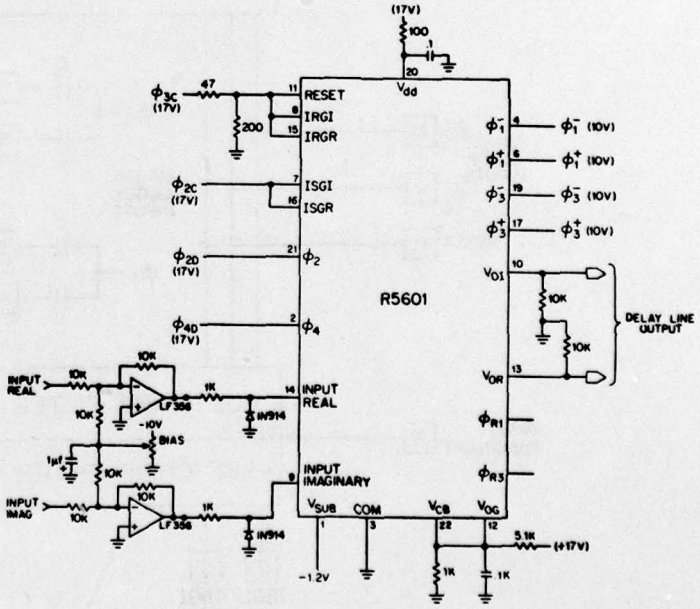


Figure 4 - Connection Arrangement for R5601.

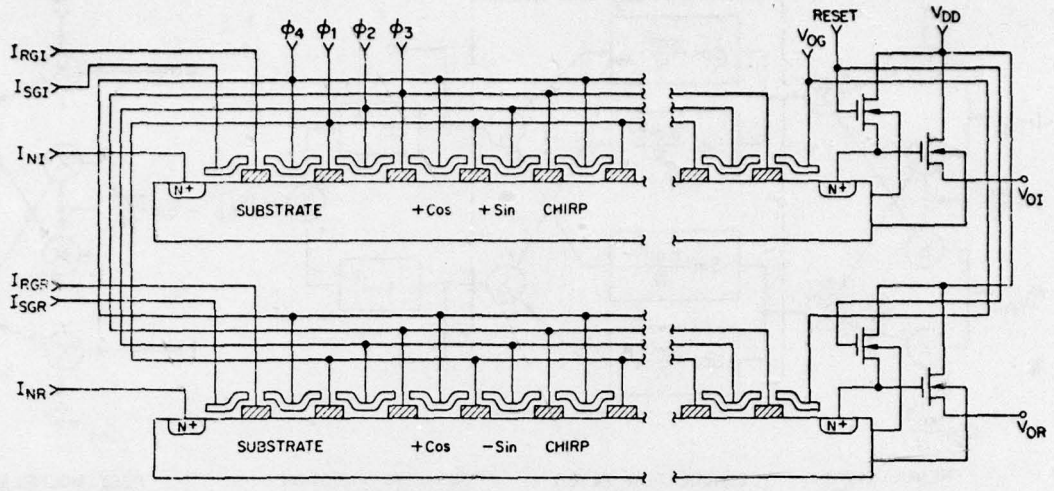


Figure 5 - Schematic layout of the CCD channels, edge view.

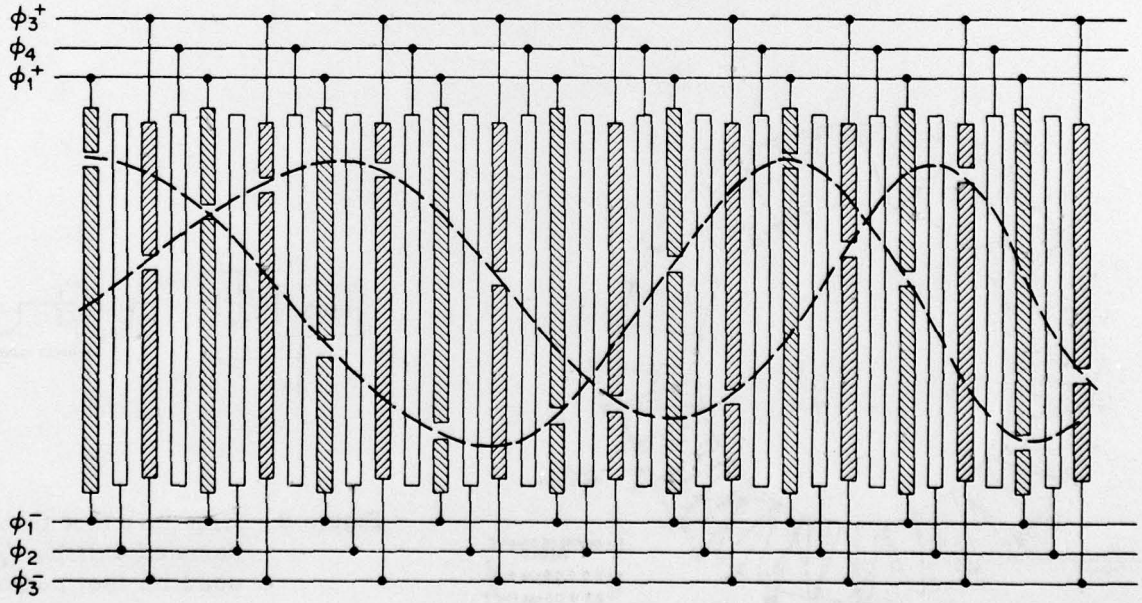


Figure 6 - Schematic layout of the CCD gates showing the split-gate weighting.

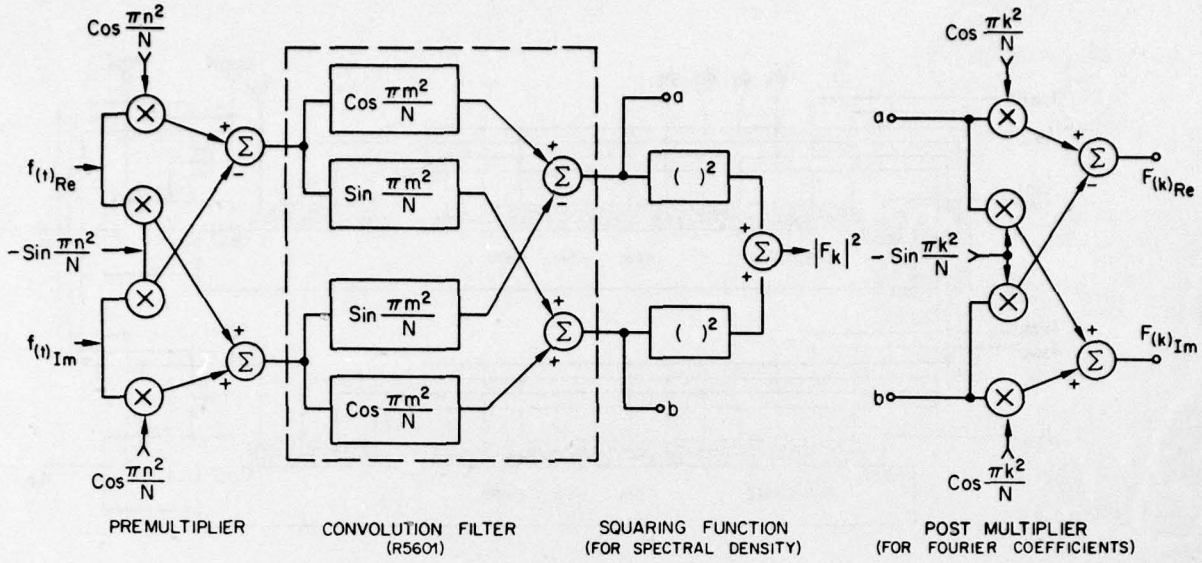


Figure 7 - Block Diagram for Implementation of DFT or Spectral Density.

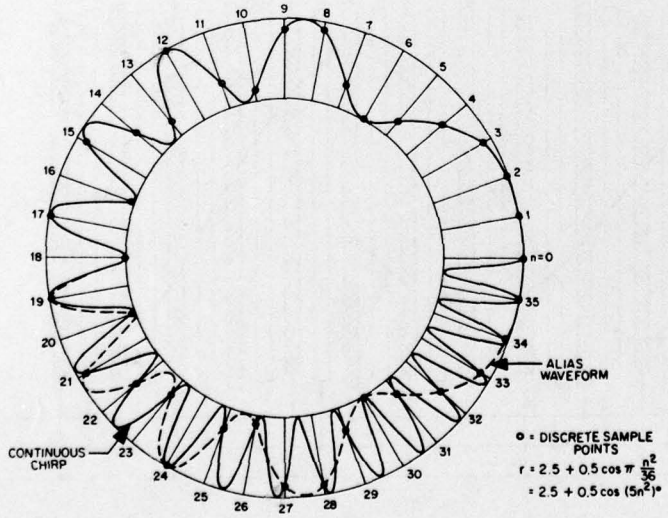


Figure 8 - Chirp Waveform

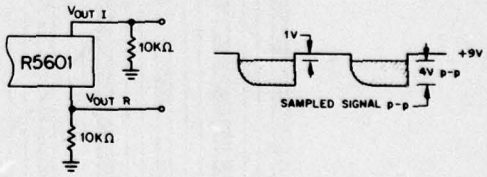
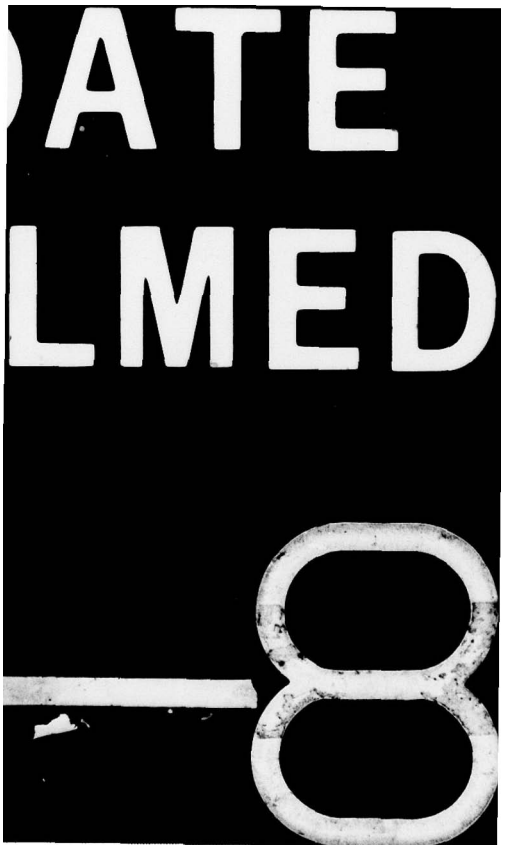


Figure 9 - Illustration of the delayed sampled output, V_{OR} or V_{OI}, used for test purposes.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